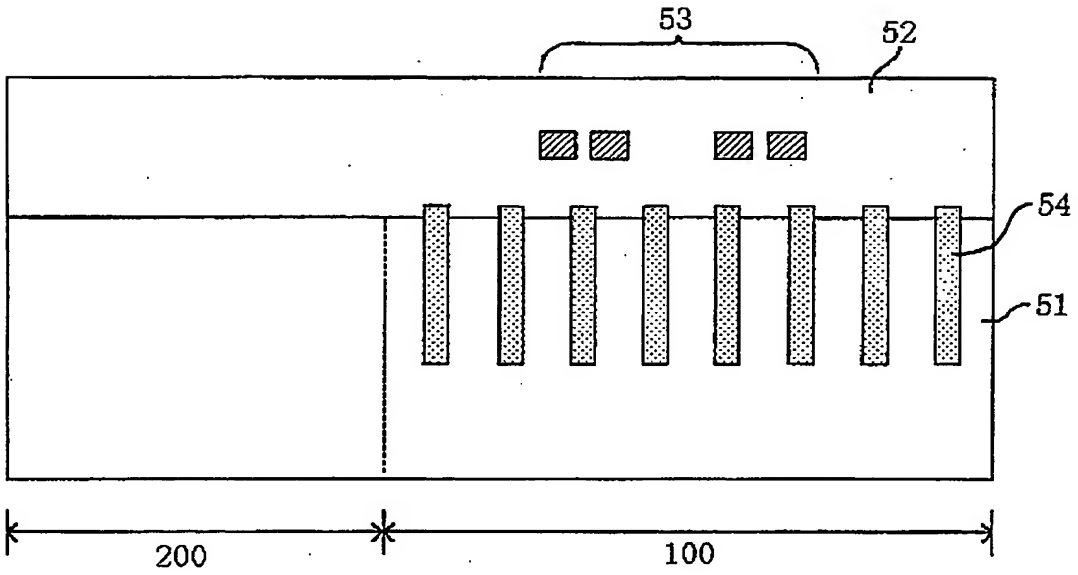
Fig. 1



51 SEMICONDUCTOR SUBSTRATE
52 LEYERED FILM
53 INDUCTOR
54 LOW-PERMITTIVITY FILLING MEMBER
100 RF CIRCUIT AREA
200 DIGITAL CIRCUIT AREA

Fig. 2

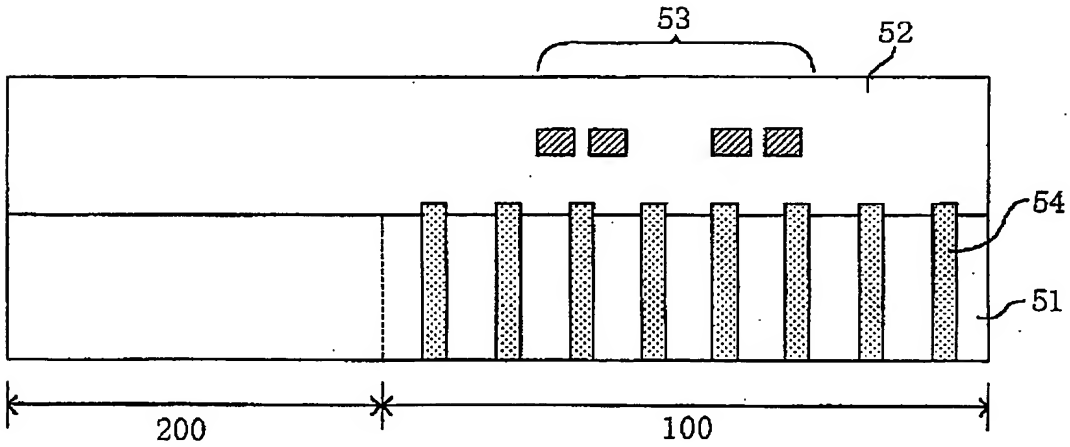


Fig. 3

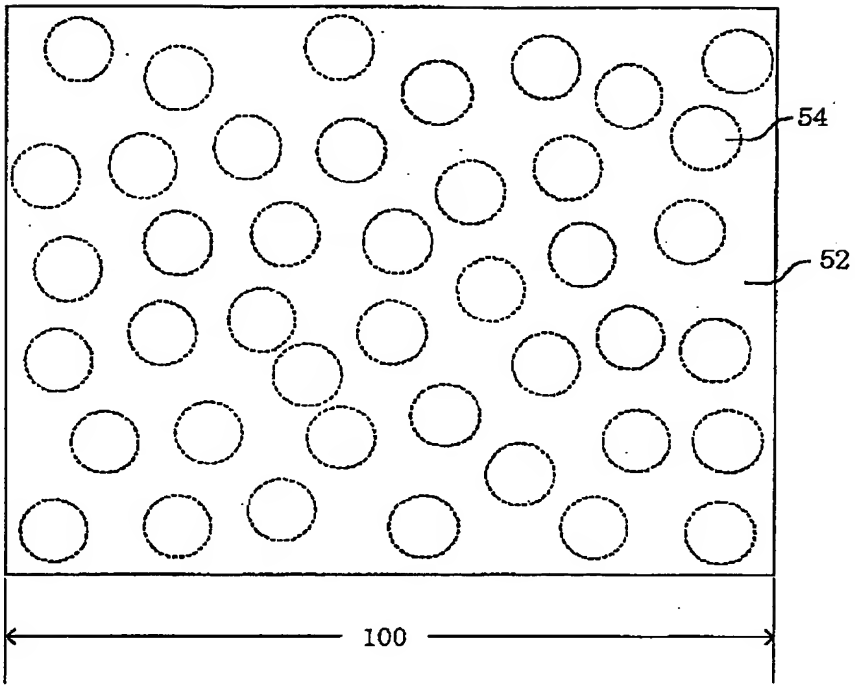


Fig. 4

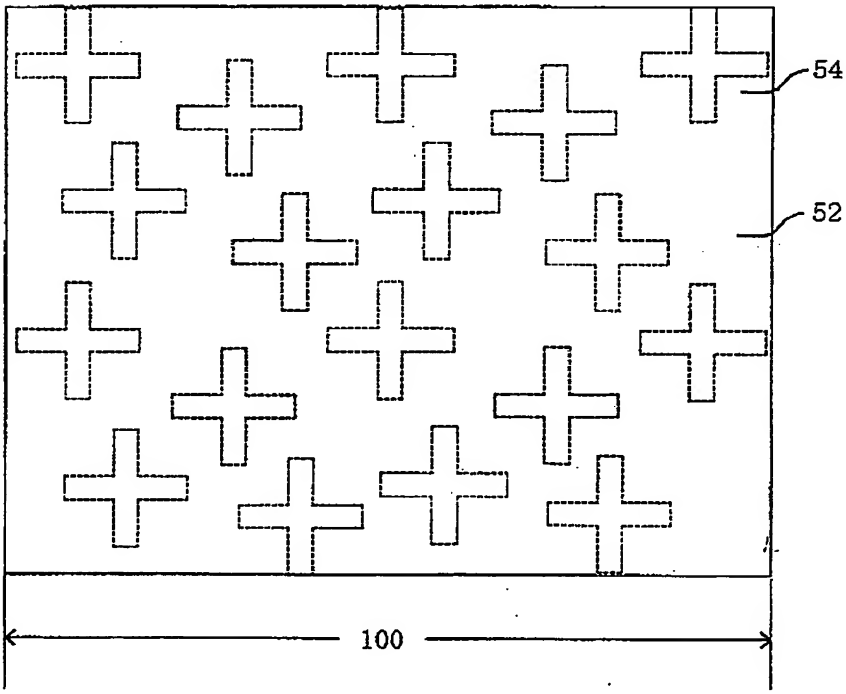
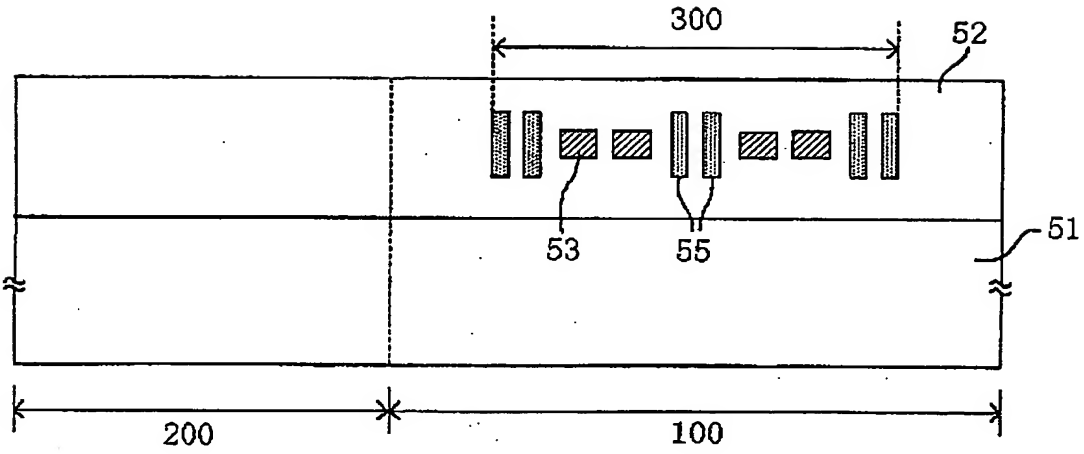
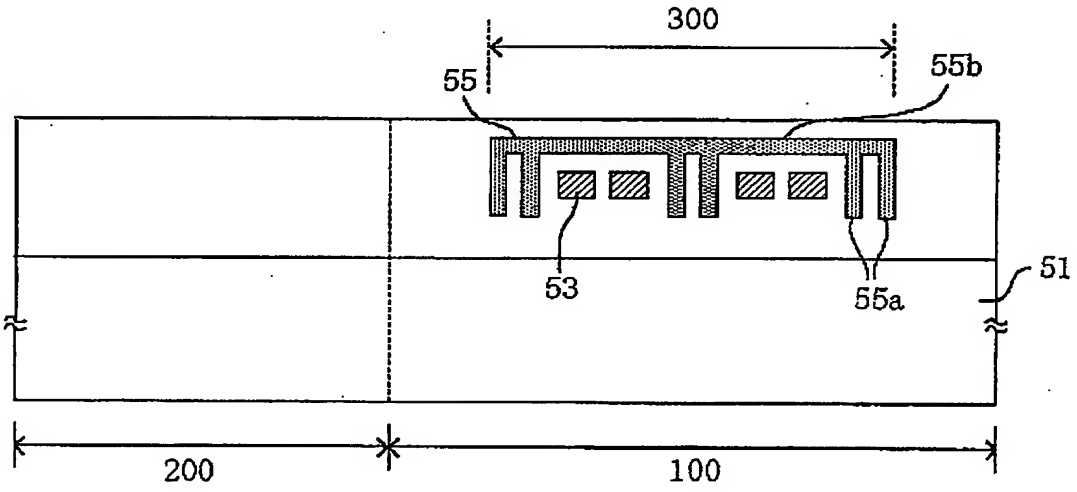


Fig. 5



55 HIGH PEMEABILITY FILLING MEMBER
300 HIGH-PERMEABILITY AREA

Fig. 6



55A ROD MEMBER
55B PLANE MEMBER

Fig. 7

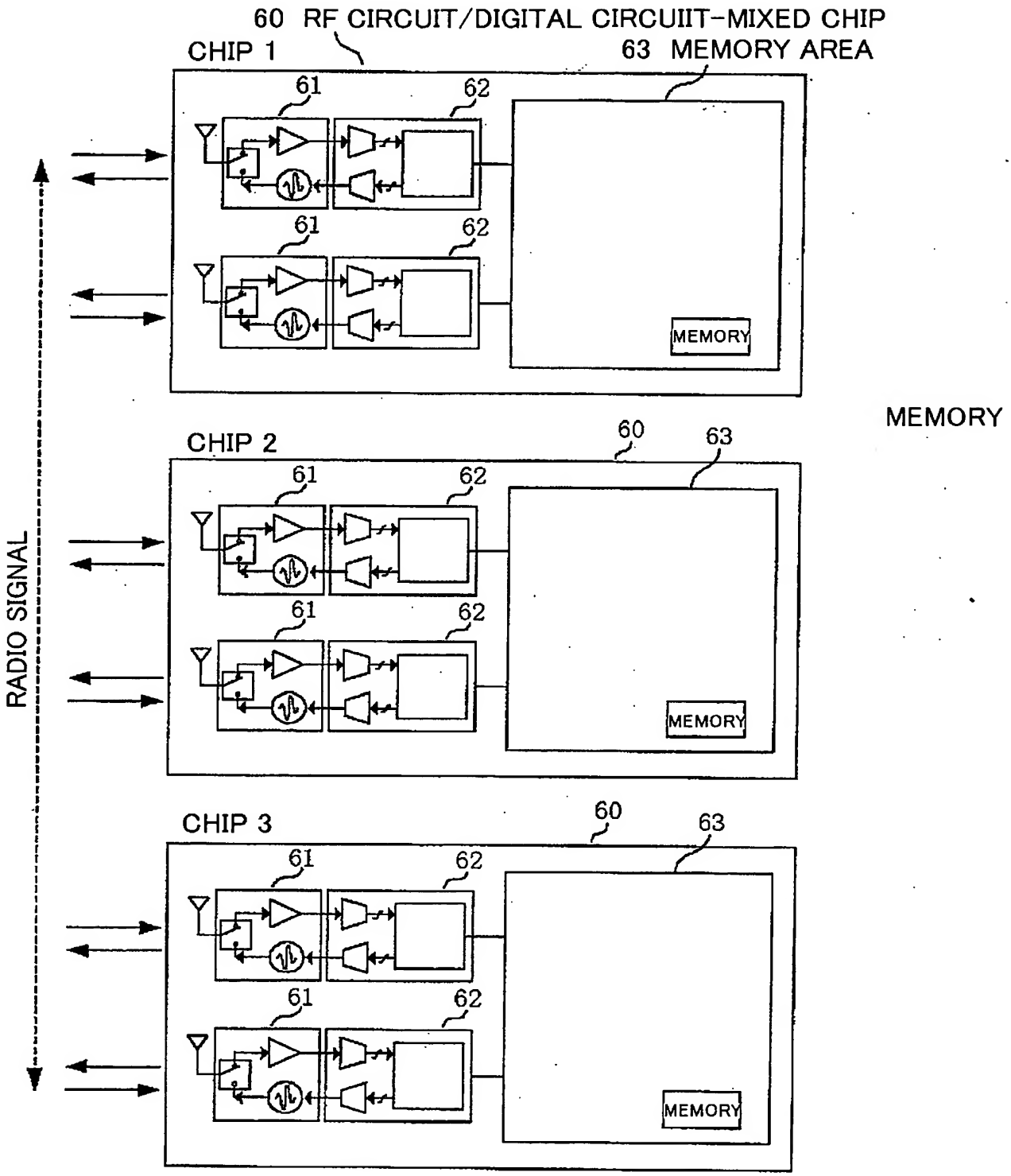

60 RF CIRCUIT/DIGITAL CIRCUIIT-MIXED CHIP
CHIP 1
63 MEMORY AREA
61
62
MEMORY
CHIP 2
60
63
CHIP 3
RADIO SIGNAL
MEMORY

Fig. 8

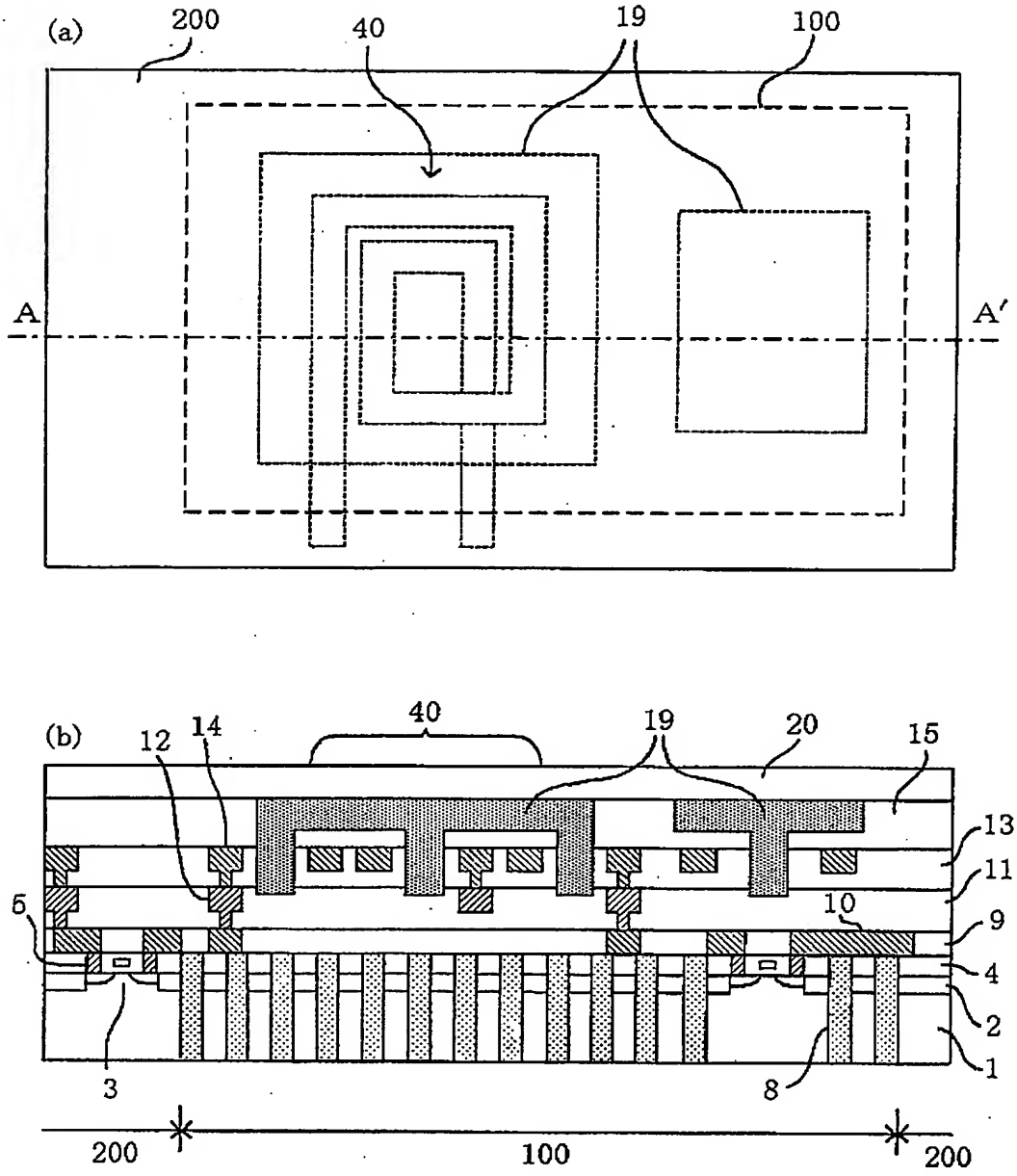


Fig. 9

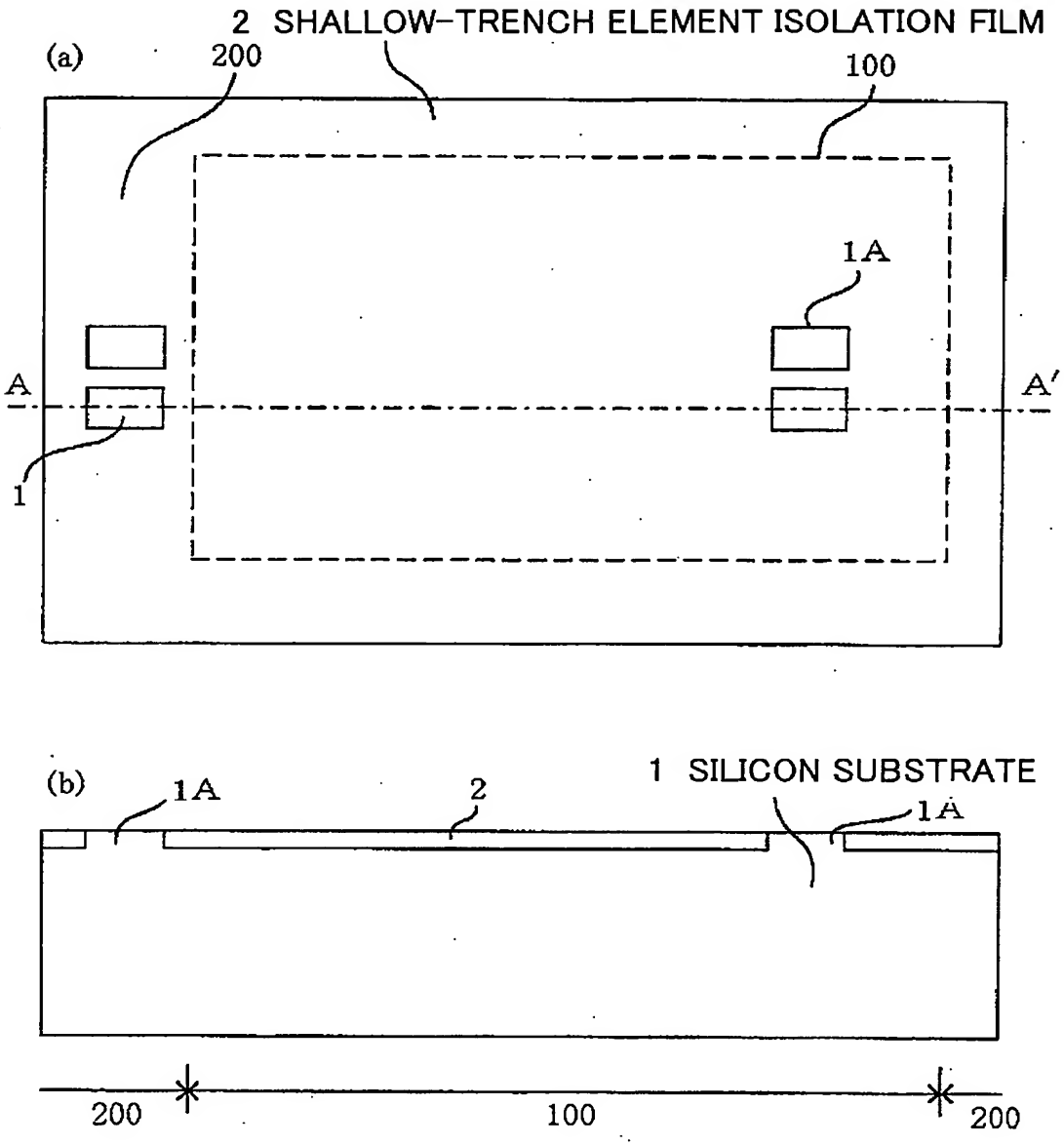

2 SHALLOW-TRENCH ELEMENT ISOLATION FILM
(a)
200
100
1A
A
A'
1
(b)
1A
2
1 SILICON SUBSTRATE
1A
200
100
200

Fig. 10

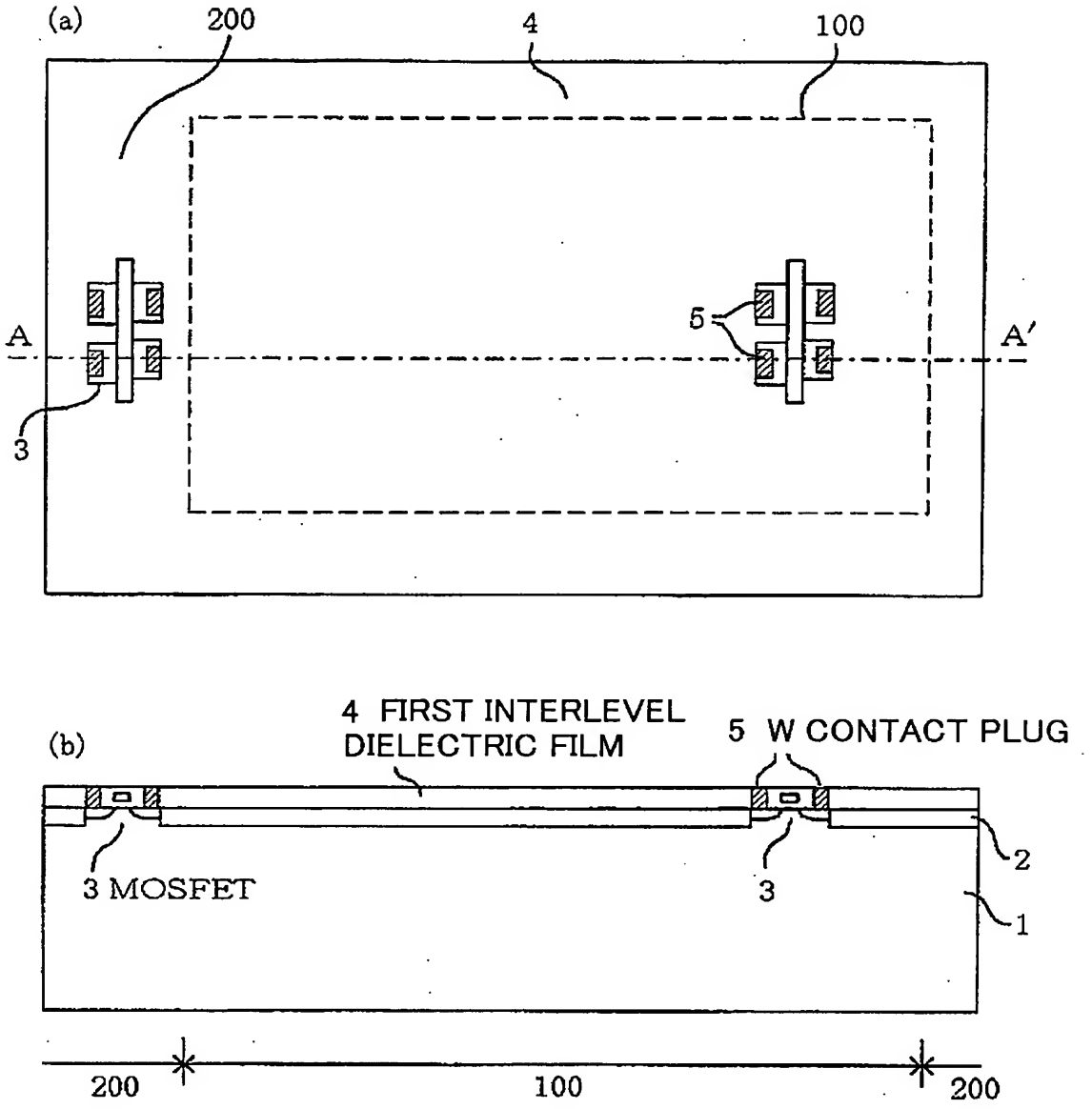

(a)
200
4
100
A
A'
5
3
(b)
4 FIRST INTERLEVEL DIELECTRIC FILM
5 W CONTACT PLUG
3 MOSFET
3
2
1
200
100
200

Fig. 11

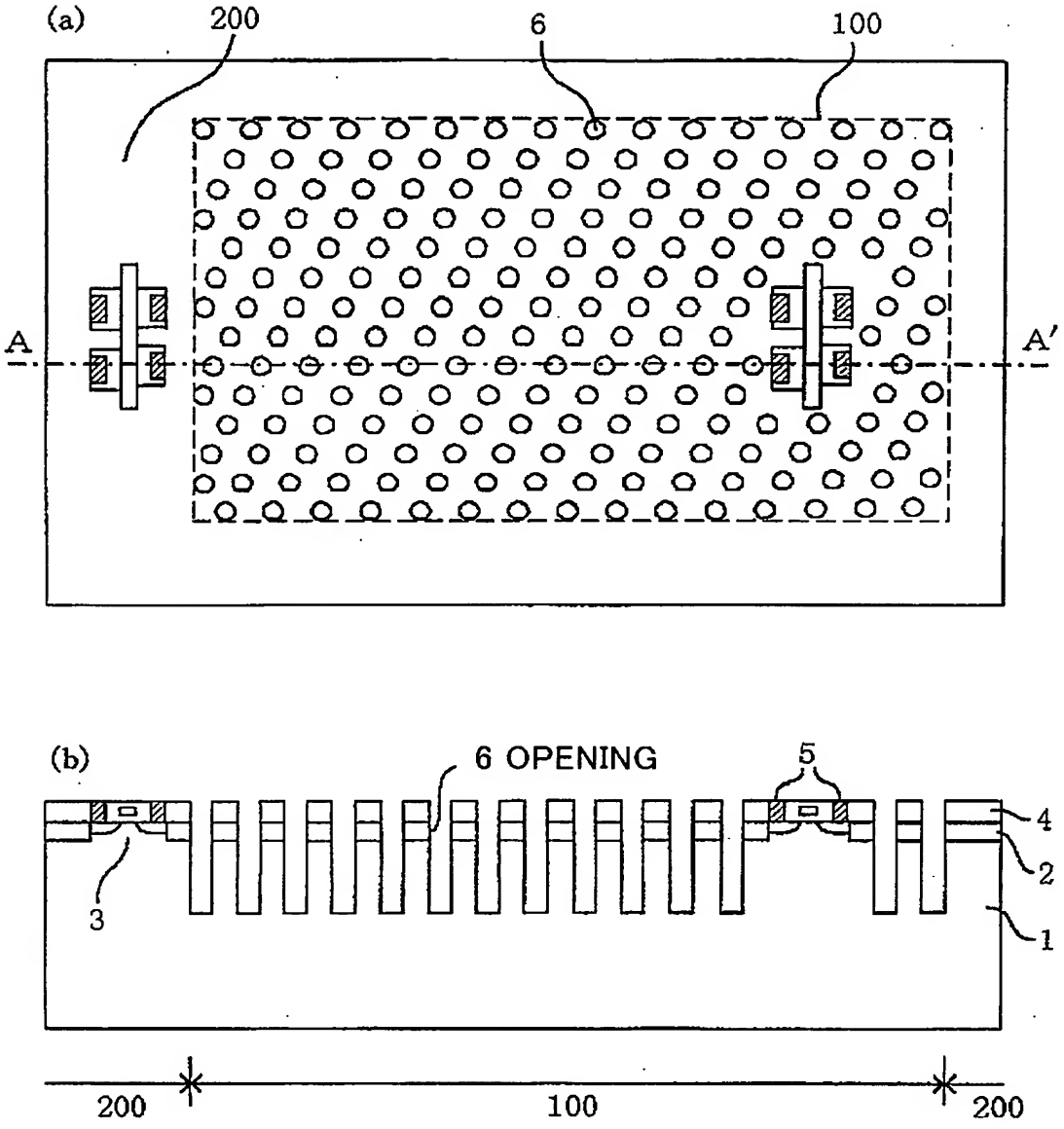


Fig. 12

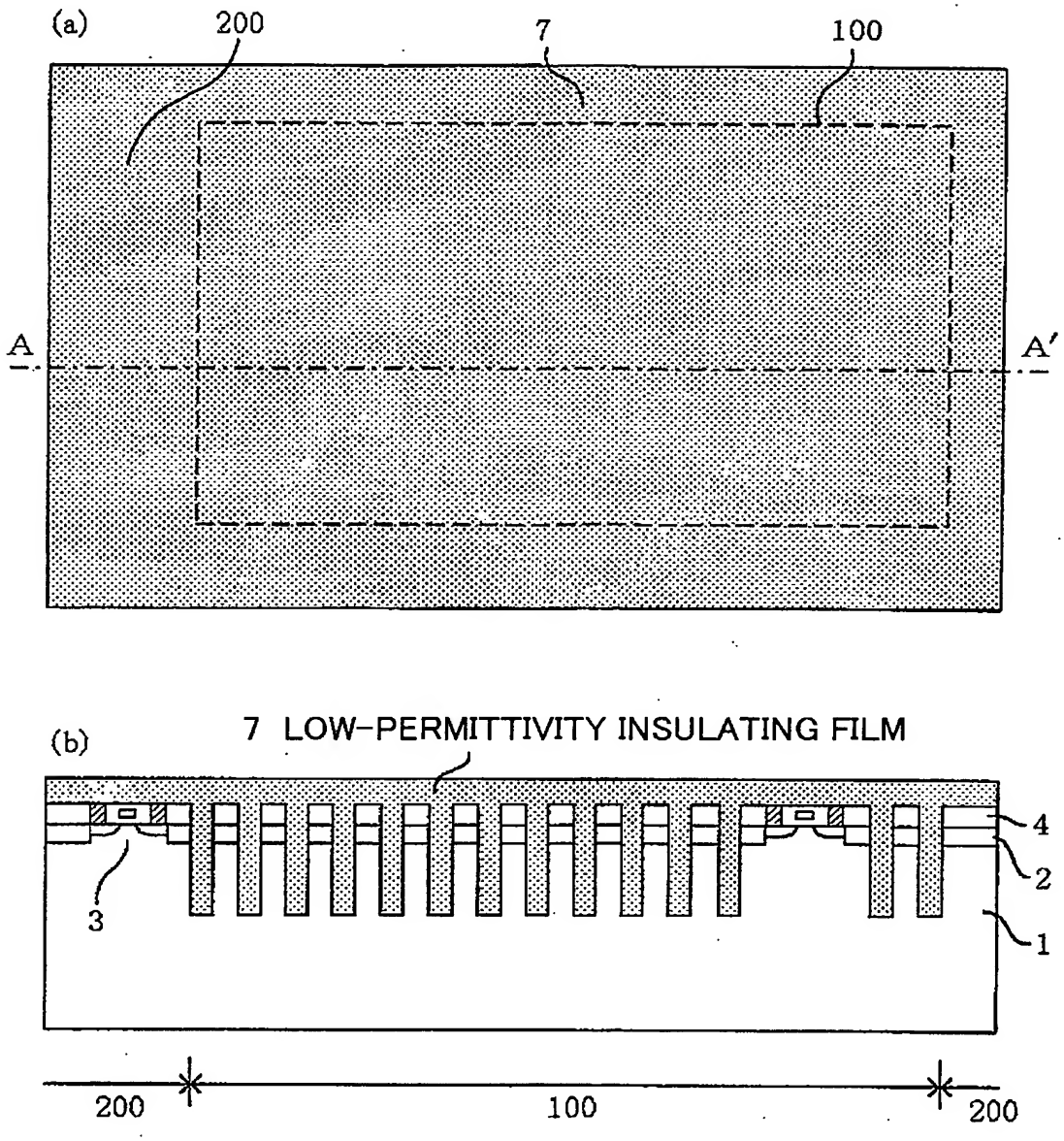

(a)
200
7
100
A
A'
(b)
7 LOW-PERMITTIVITY INSULATING FILM
4
2
1
3
200
100
200

Fig. 13

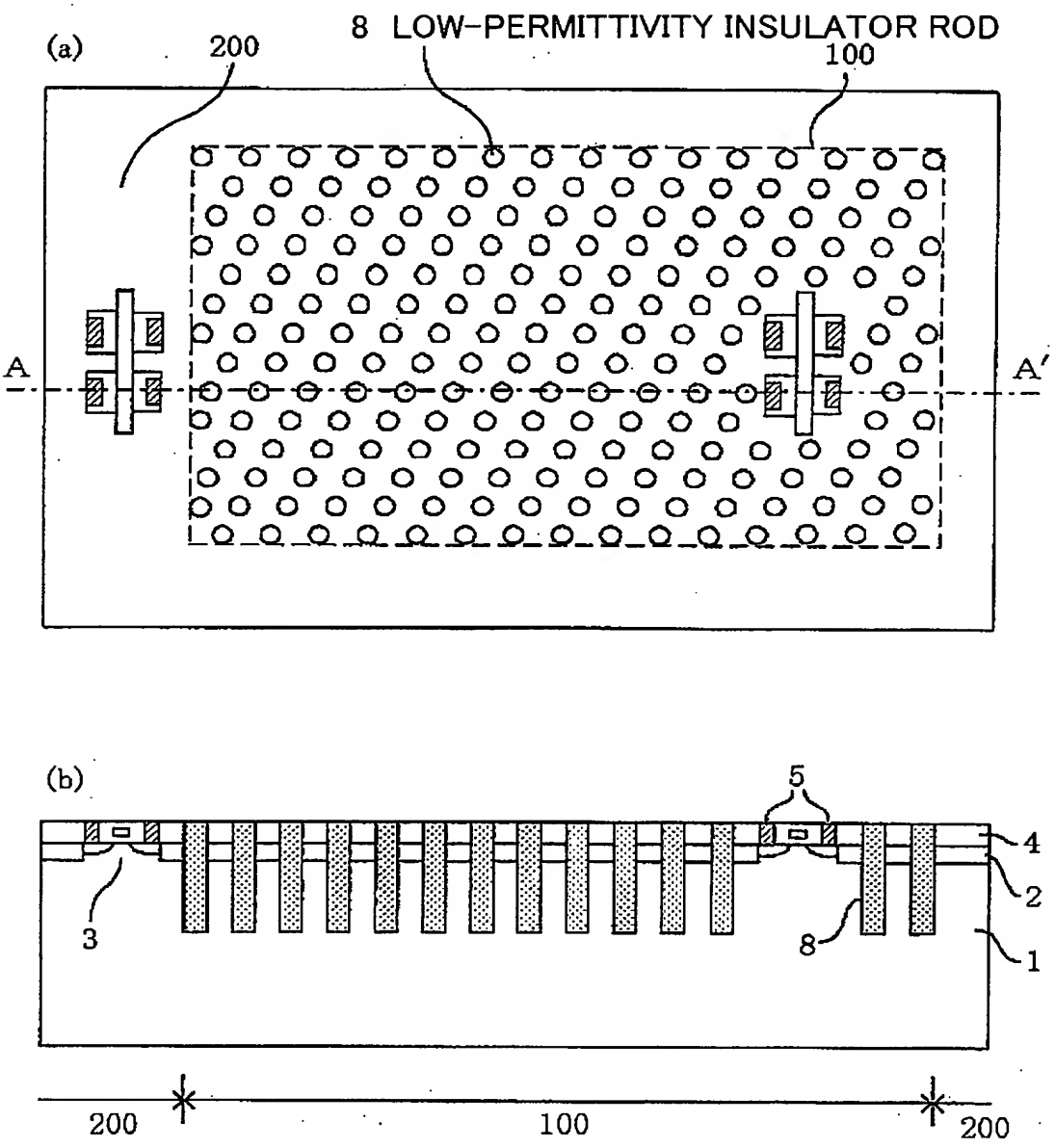

(a)
200
8 LOW-PERMITTIVITY INSULATOR ROD
100
A
A'
(b)
5
4
2
3
8
1
200
100
200

Fig. 14

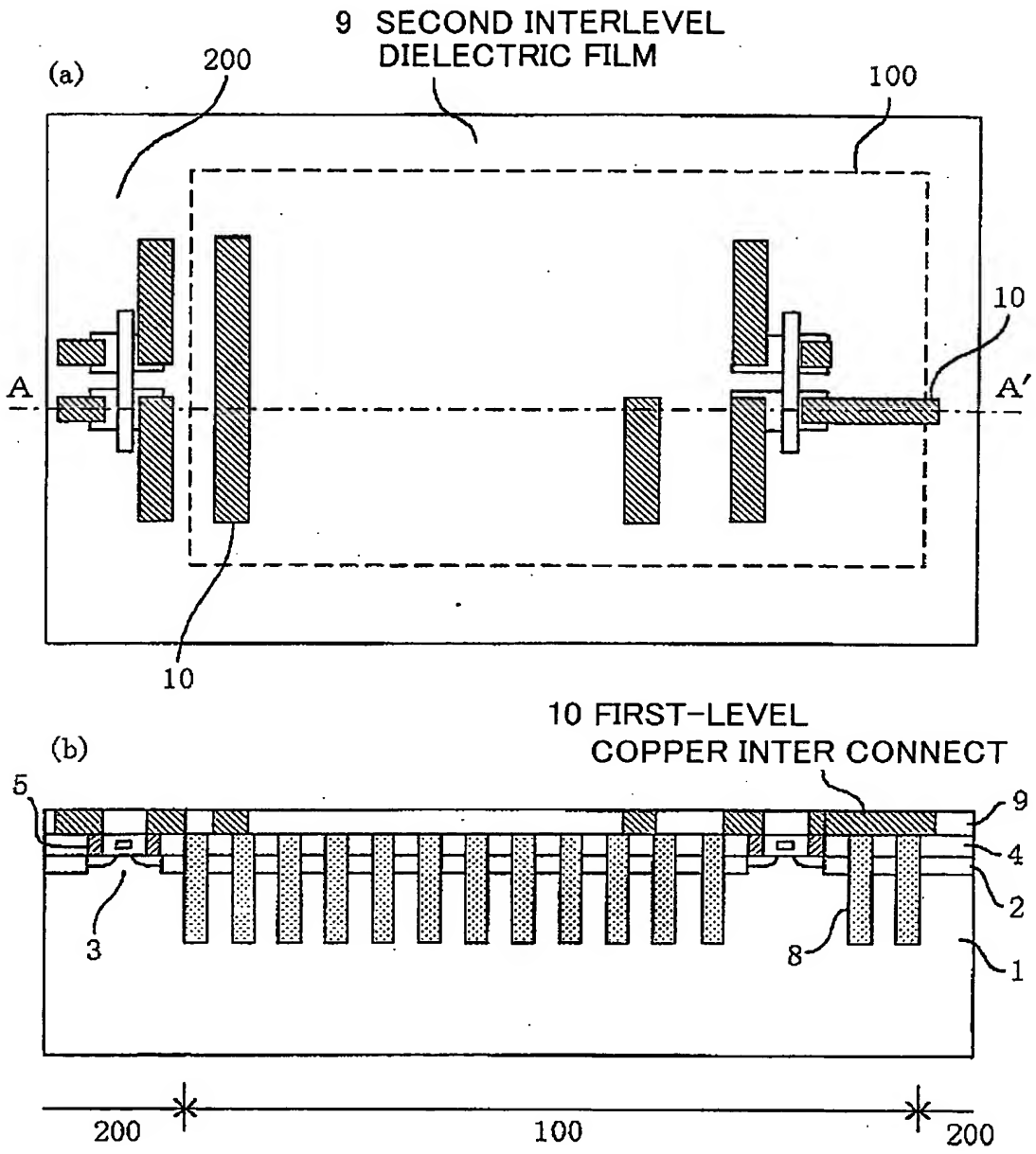
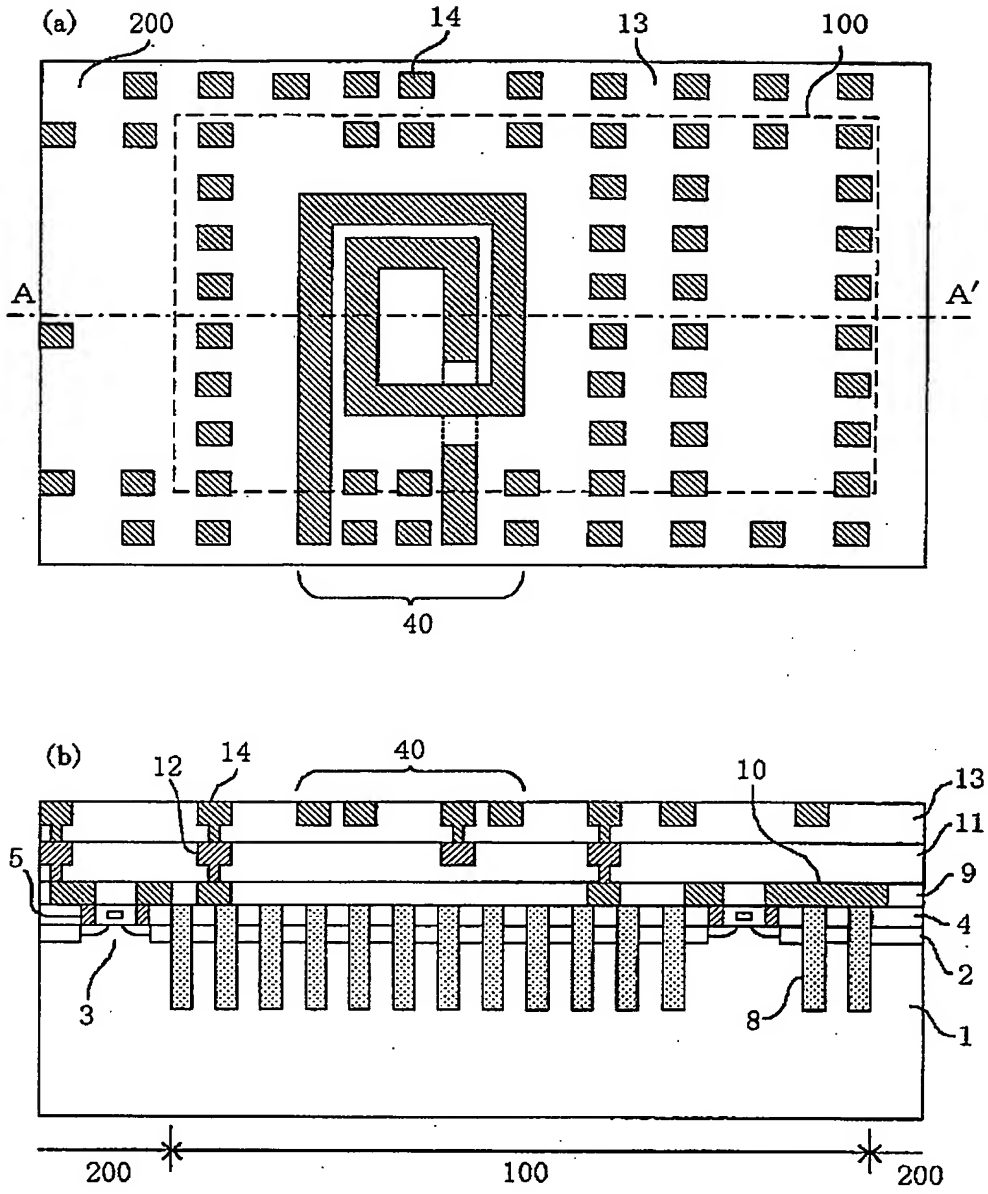
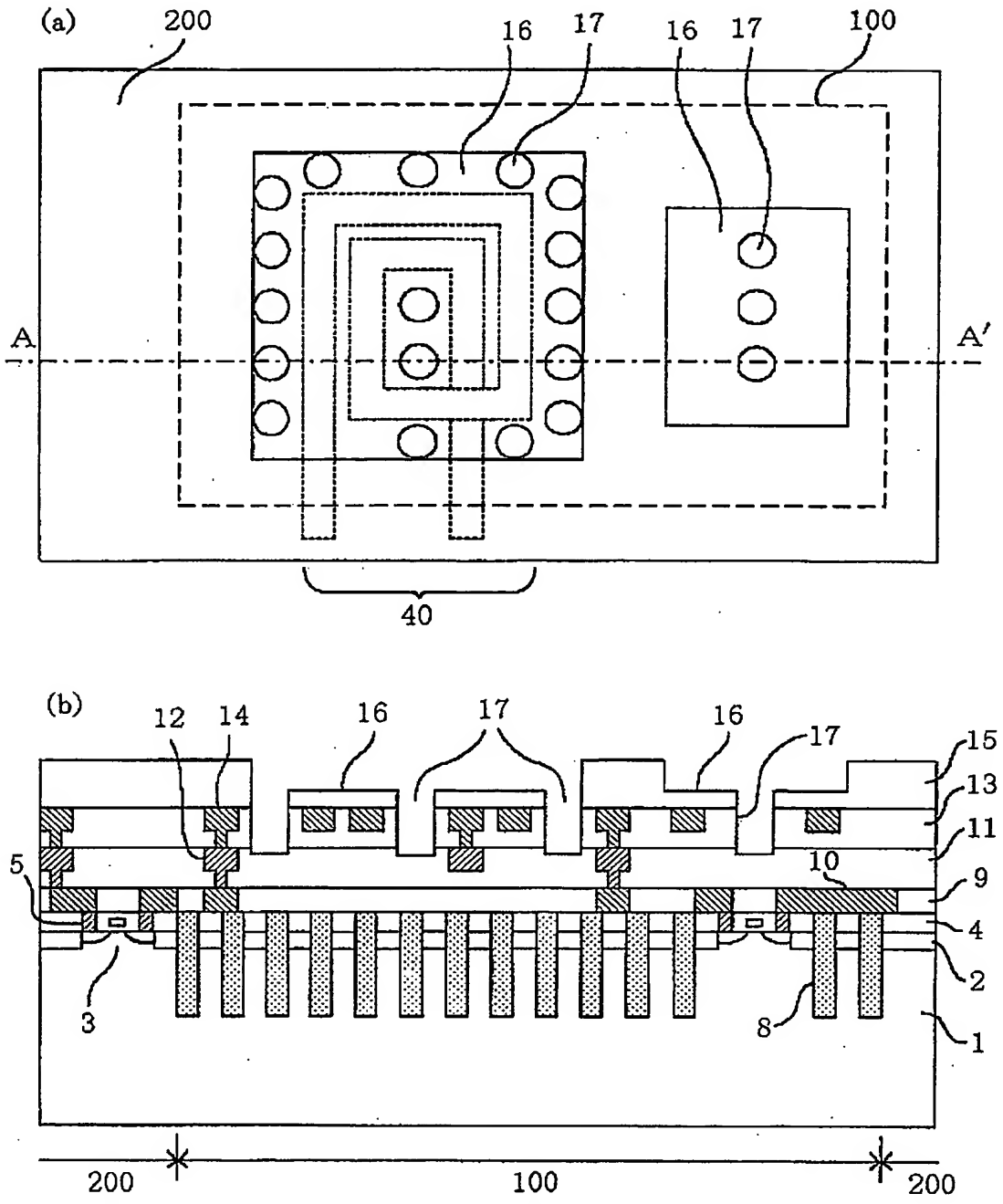

9 SECOND INTERLEVEL DIELECTRIC FILM
(a)
200
100
10
A
A'
10
10 FIRST-LEVEL COPPER INTER CONNECT
(b)
5
9
4
2
1
3
8
200
100
200

Fig. 15



11 THIRD INTERLEVEL DIELECTRIC FILM
12 SECOND INTERLEVEL DIELECTRIC FILM
13 FOURTH INTERLEVEL DIELECTRIC FILM
14 THIRD-LEVEL COPPER INTERCONNECT
40 INDUCTOR

Fig. 16



15 FIFTH INTERLEVEL DIELECTRIC FILM
16 DEPRESSION
17 OPENING

Fig. 17

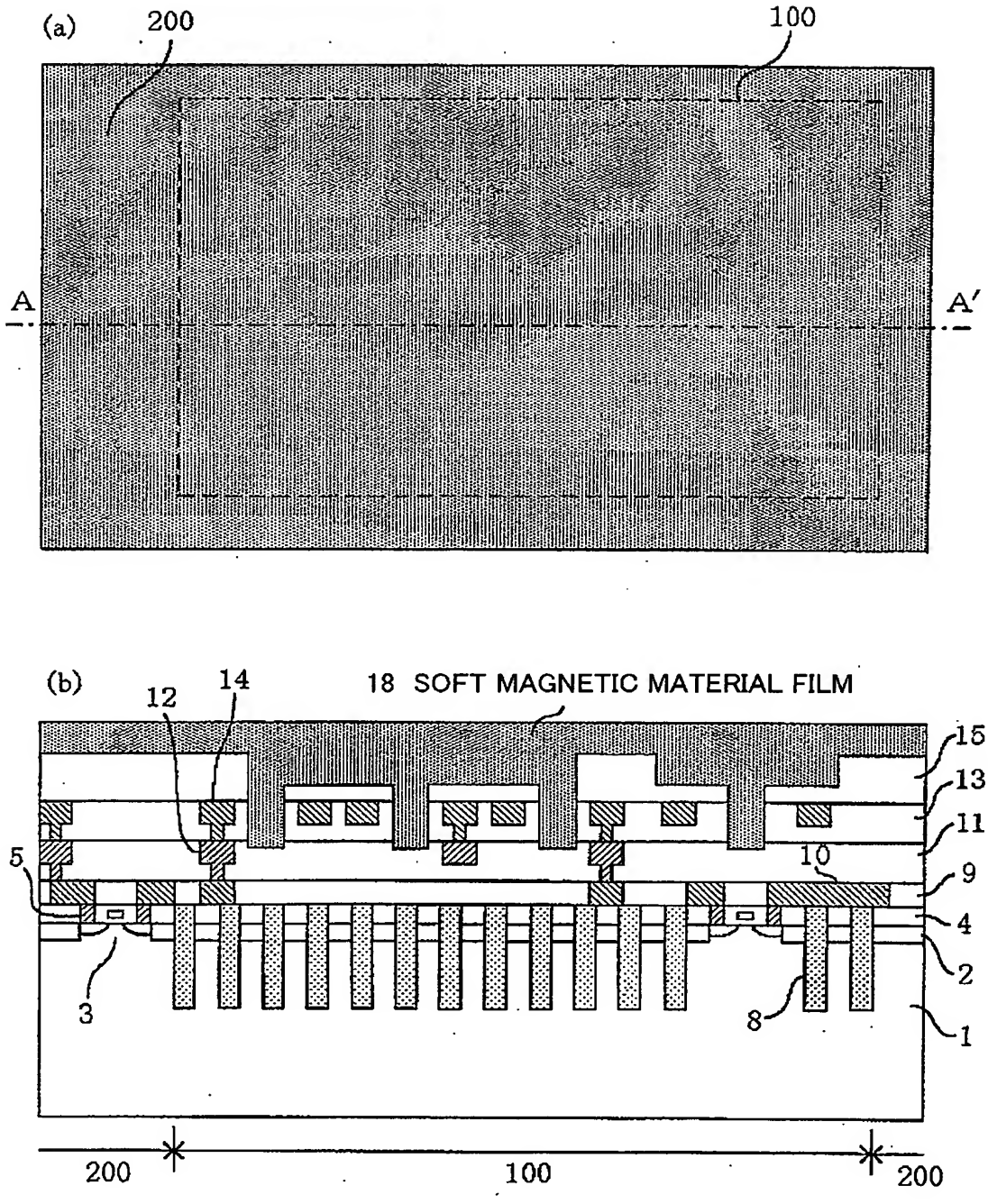

(a)
200
100
A
A'
(b)
18 SOFT MAGNETIC MATERIAL FILM
12
14
15
13
11
10
9
5
4
2
3
8
1
200
100
200

Fig. 18

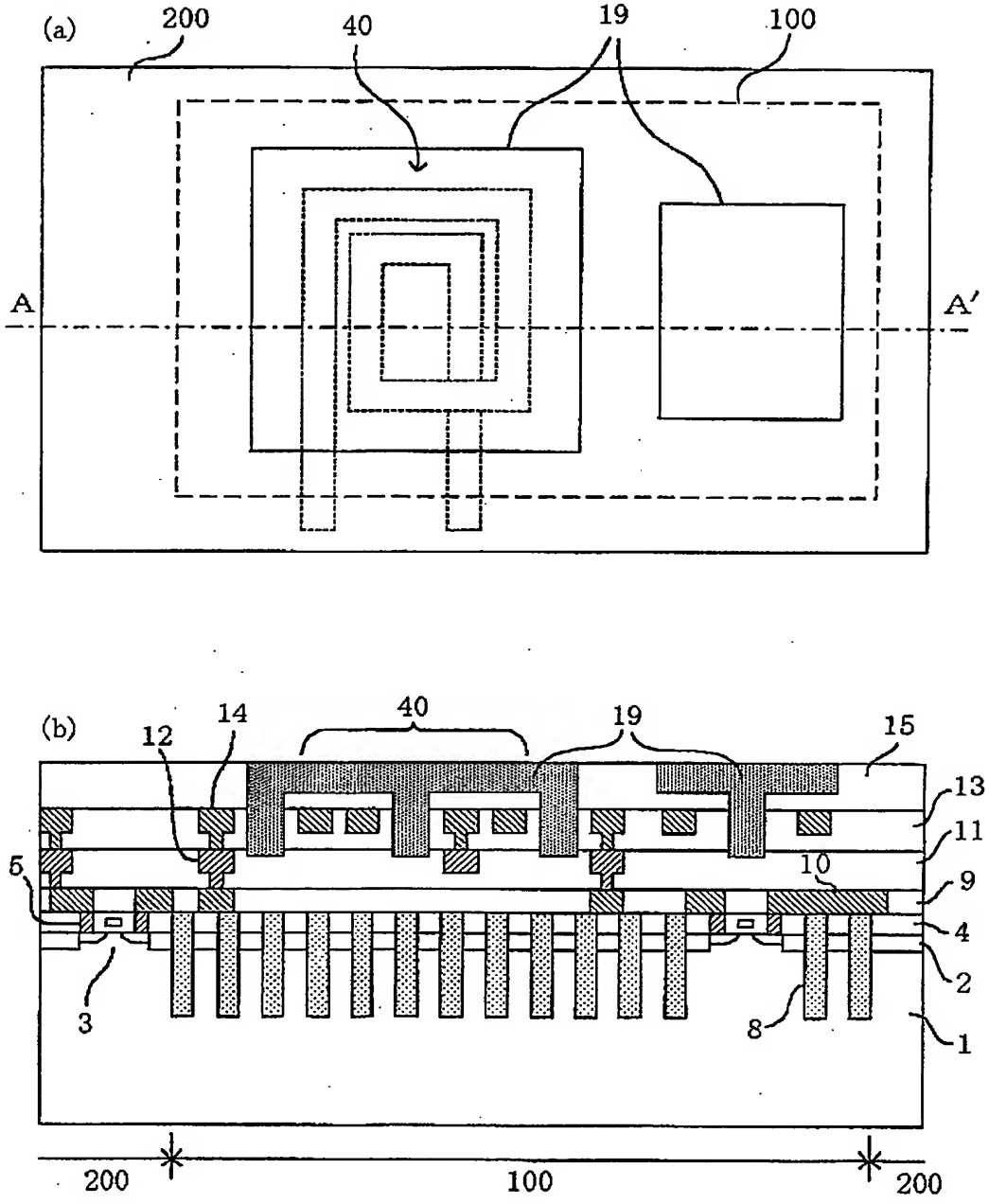
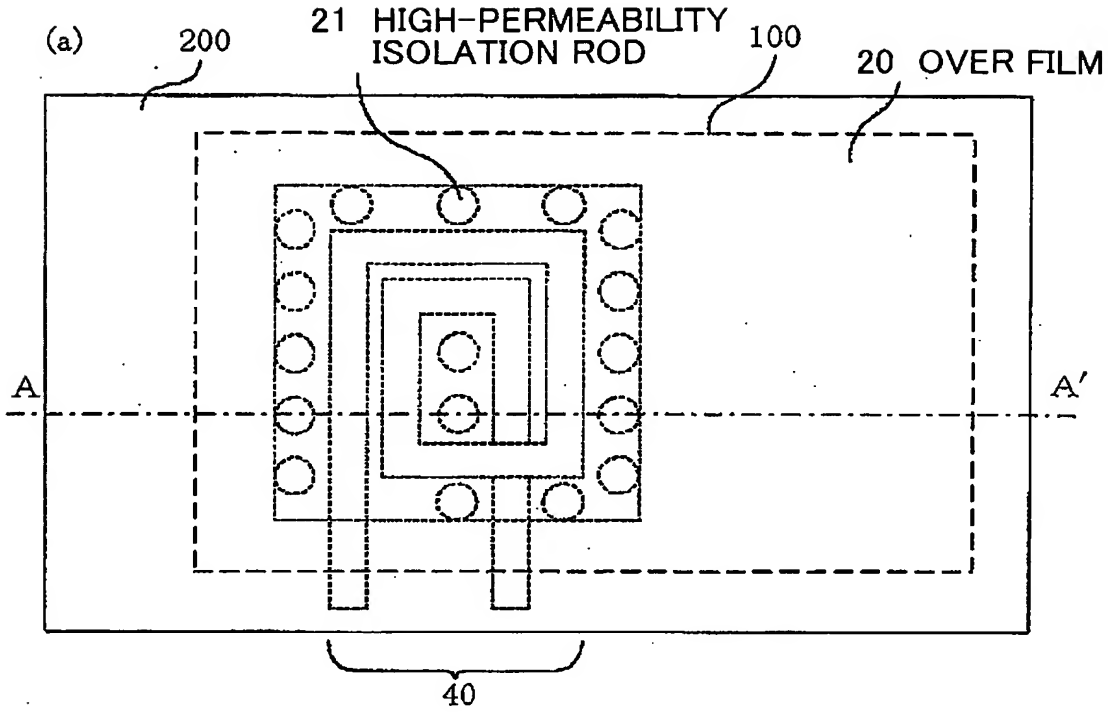


Fig. 19


(a)
200
21 HIGH-PERMEABILITY ISOLATION ROD
100
20 OVER FILM
A
A'
40

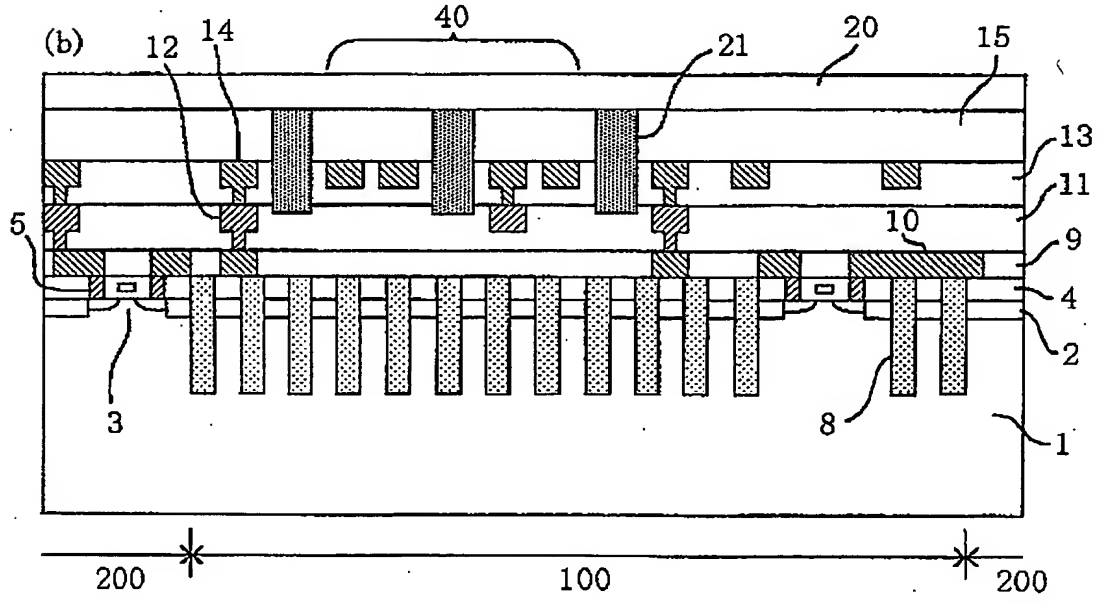
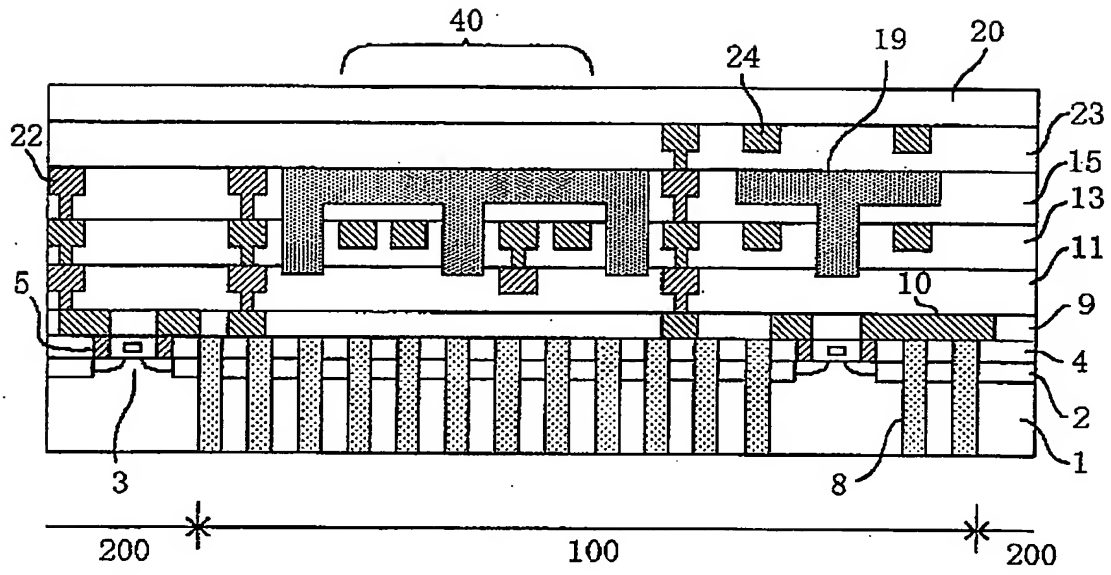
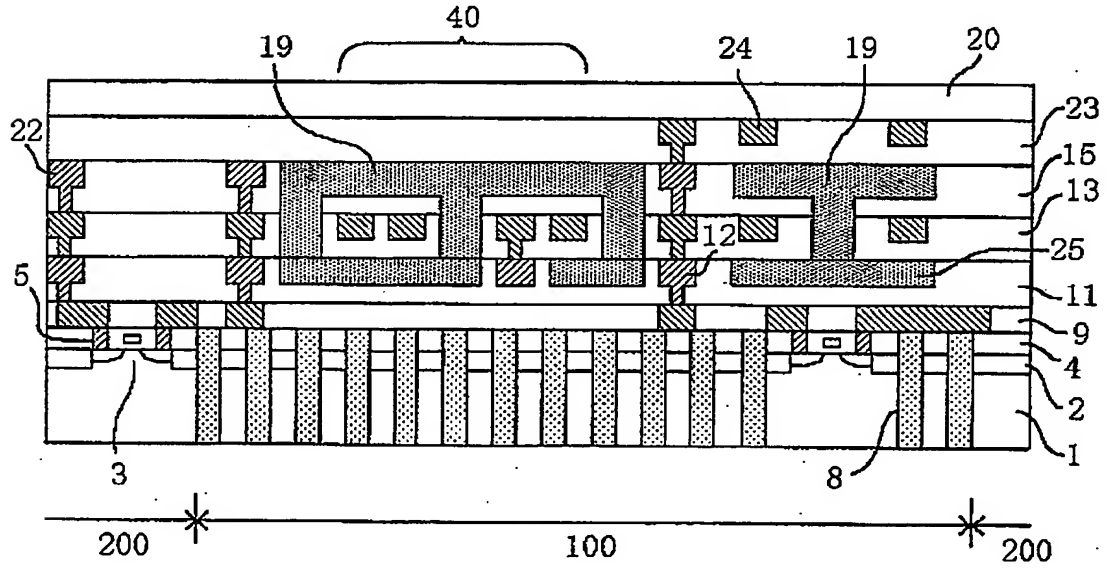

(b)
40
12
14
21
20
15
13
11
10
9
5
4
2
3
8
1
200
100
200

Fig. 20



22 FOURTH-LEVEL COPPER INTERCONNECT
23 SIXTH INTERLEVEL DIELECTRIC FILM

Fig. 21



24 FIFTH-LEVEL COPPER INTERCONNECT
25 HIGH-PERMEABILITY ISOLATION PLANE

Fig. 22

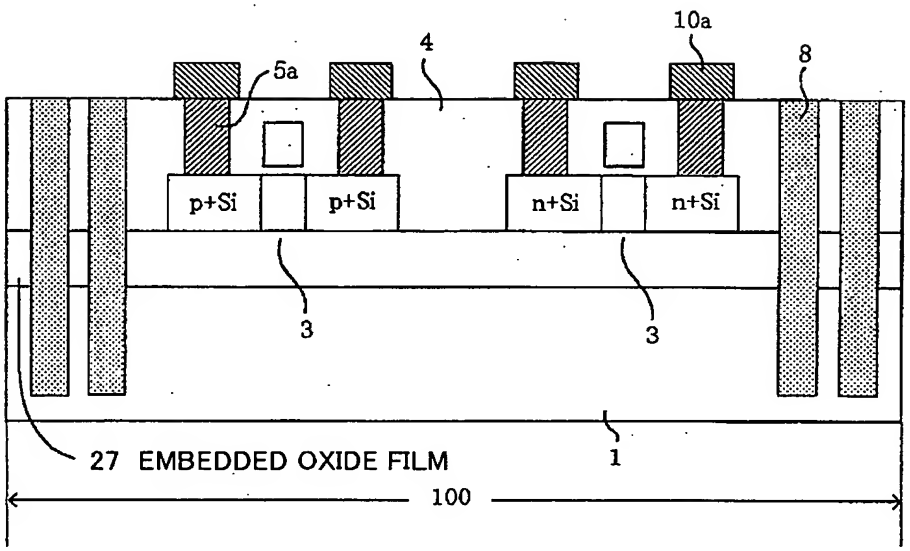
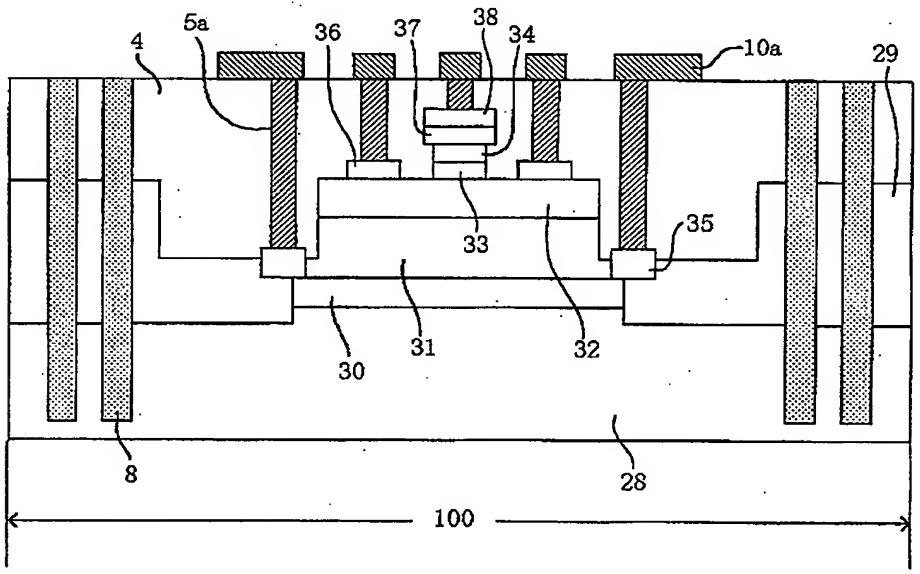
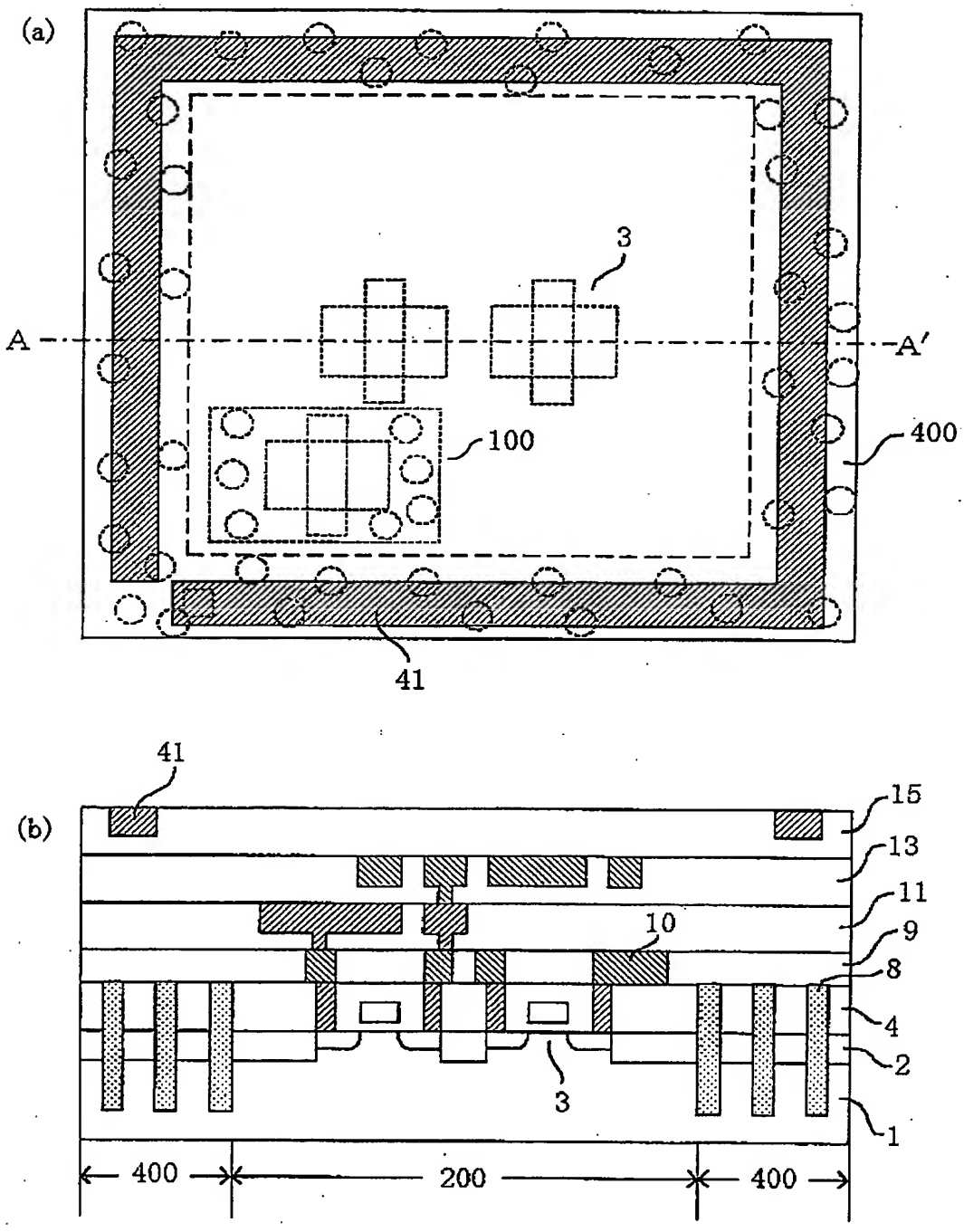


Fig. 23



28 SEMI-INSULATING GAAS SUBSTRATE
29 H^+-DOPED HIGH RESISTANCE AREA
30 N^+-GAAS LAYER
31 N^--GAAS LAYER
32 P^+-GAAS LAYER
33 N -ALGAAS LAYER
34 N-INGAAS LAYER
35 AU/NI/AUGE LAYER
36, 38 AU/PT LAYER
37 WSI LAYER

Fig. 24



41 ON-CHIP ANTENNA INTERCONNECT
400 PERIPHERAL HIGH-RESISTANCE AREA

Fig. 25

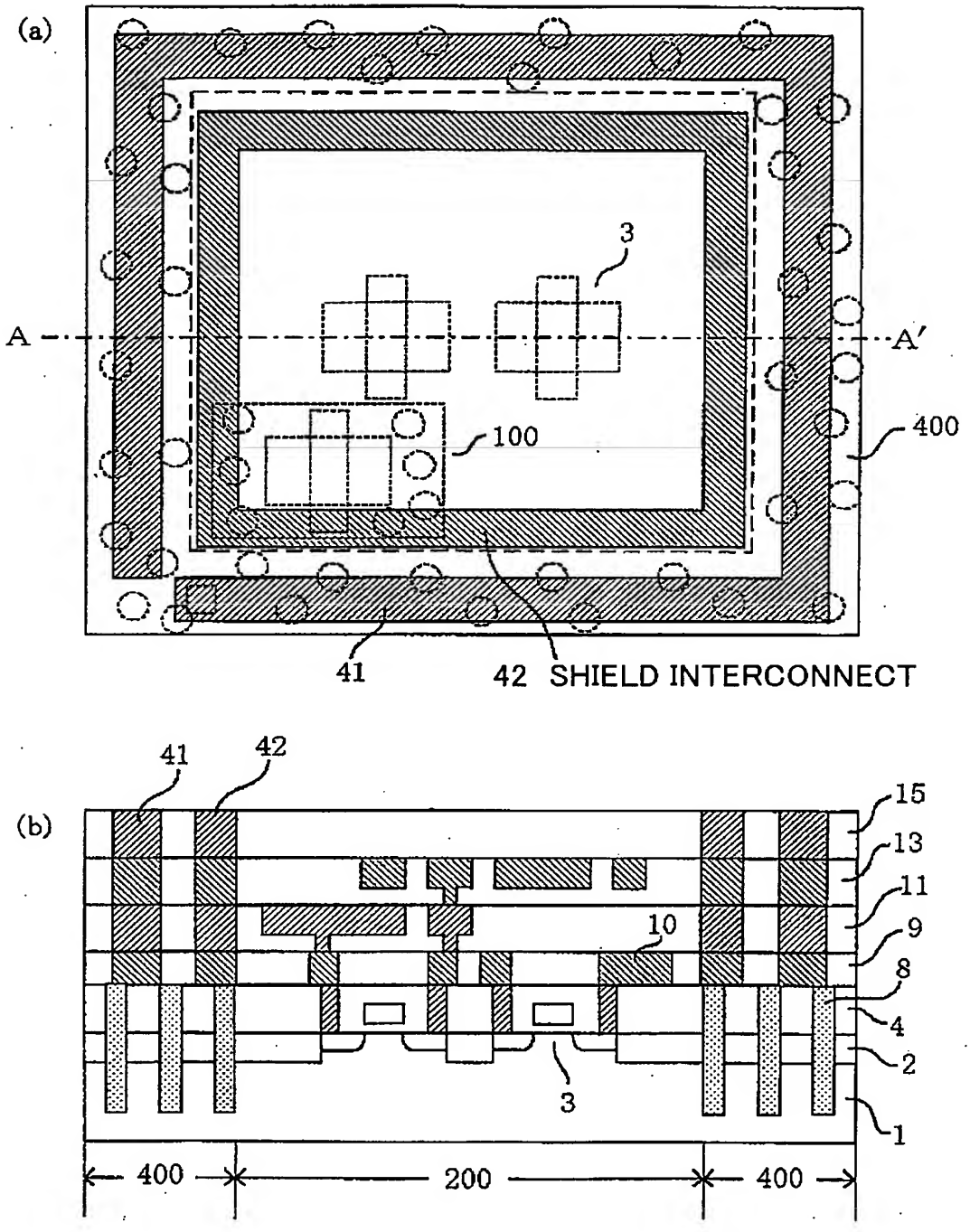
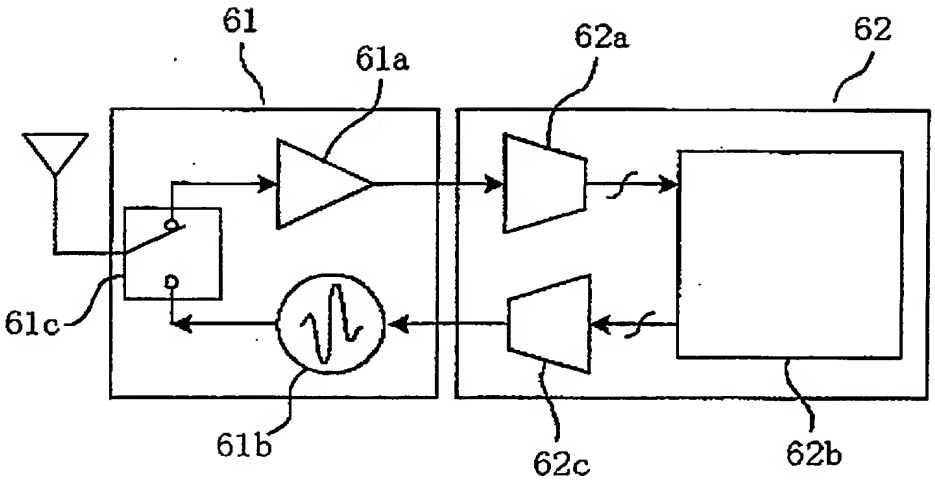

(a)
A
A'
3
100
400
41
42
SHIELD INTERCONNECT
(b)
41
42
15
13
11
10
9
8
4
2
3
1
400
200
400

Fig. 26



61 RF COMMUNICATION CIRCUIT AREA
61A LNA
61B TRANSMISSION SIGNAL GENERATING CIRCUIT
61C SWITCH CIRCUIT
62 DIGITAL BASEBAND
62A A/D CIRCUIT
62B DIGITAL SIGNAL PROCESSING CIRCUIT
63C D/A CIRCUIT

Fig. 27

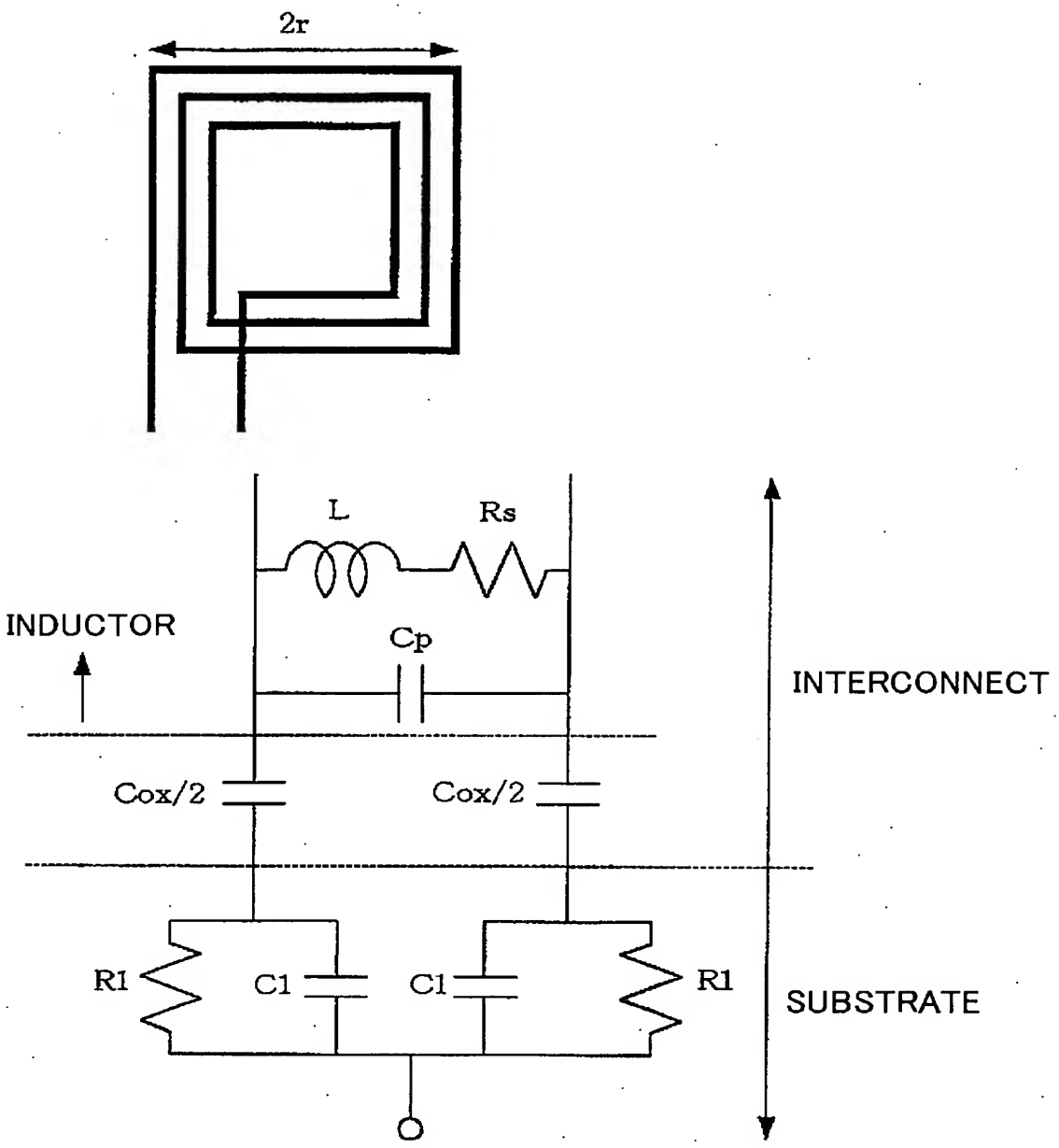

2r
L
Rs
INDUCTOR
Cp
INTERCONNECT
Cox/2
Cox/2
R1
C1
C1
R1
SUBSTRATE

Fig. 28

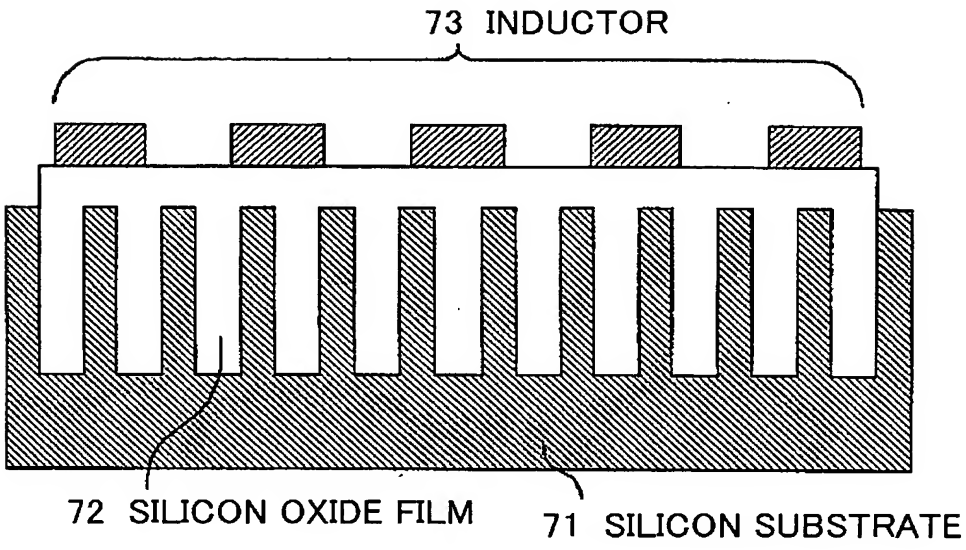


Fig. 29

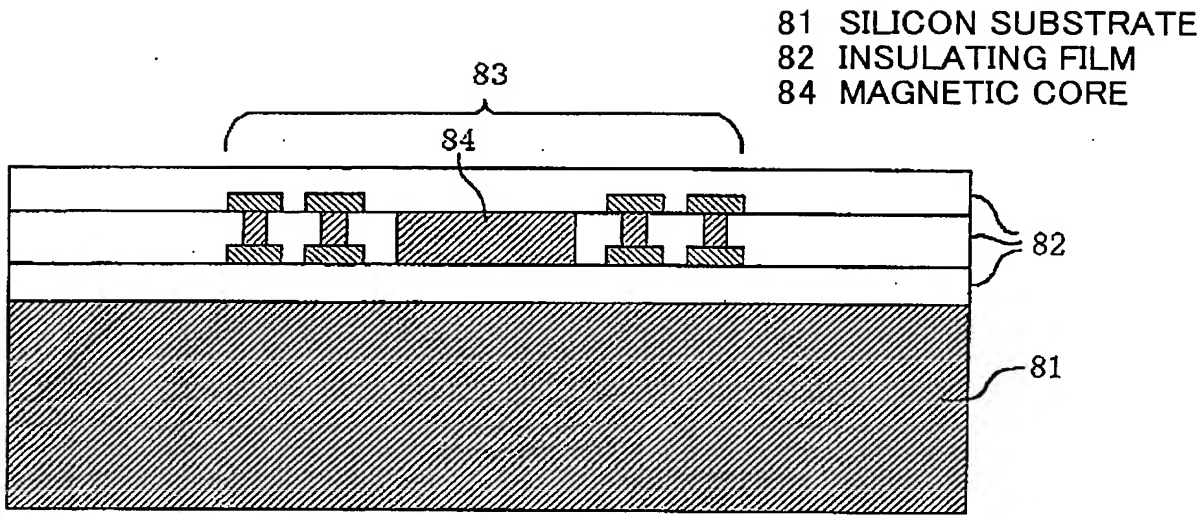

81 SILICON SUBSTRATE
82 INSULATING FILM
84 MAGNETIC CORE
83
84
82
81

Fig. 30

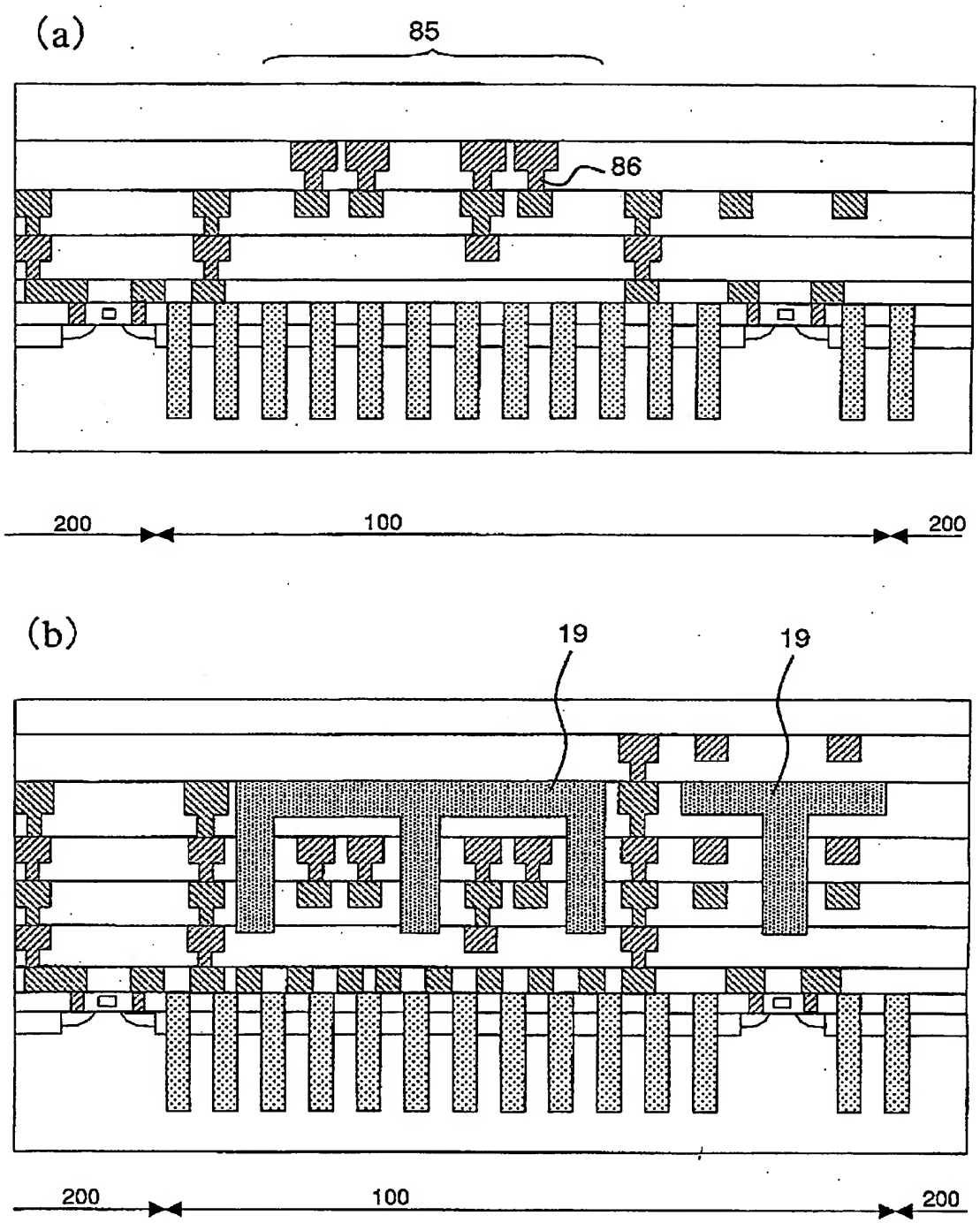


Fig. 31

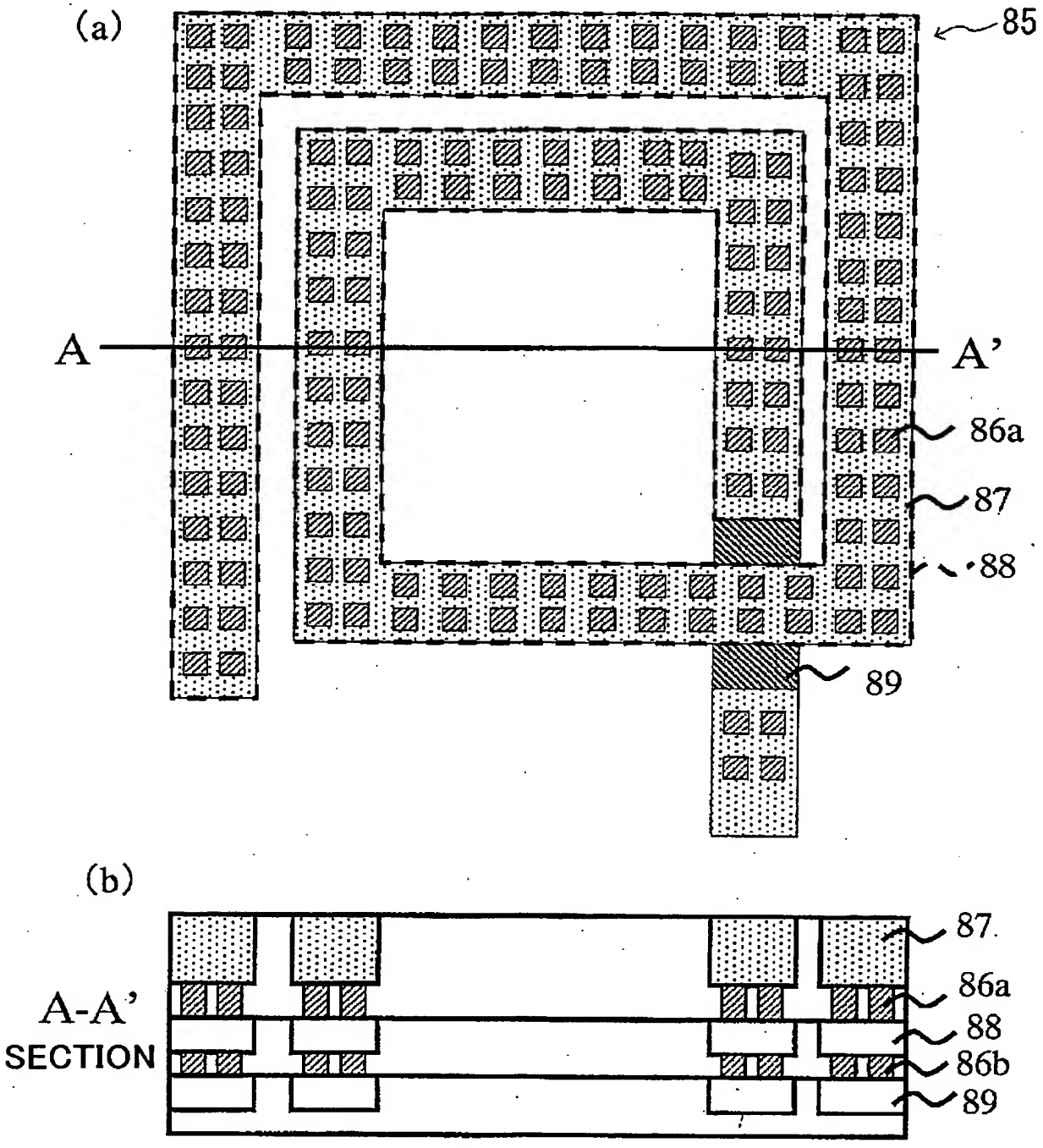


Fig. 32

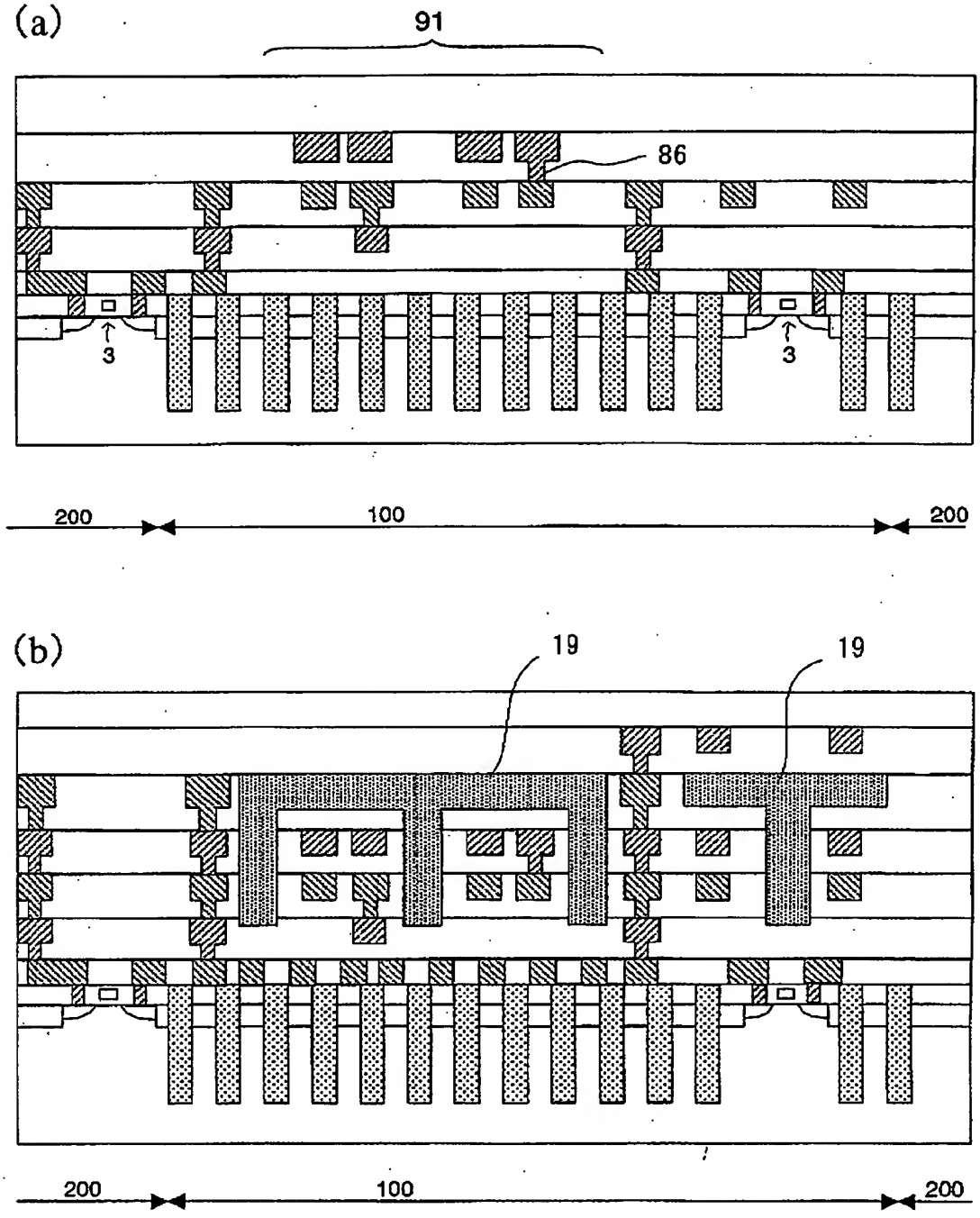


Fig. 33

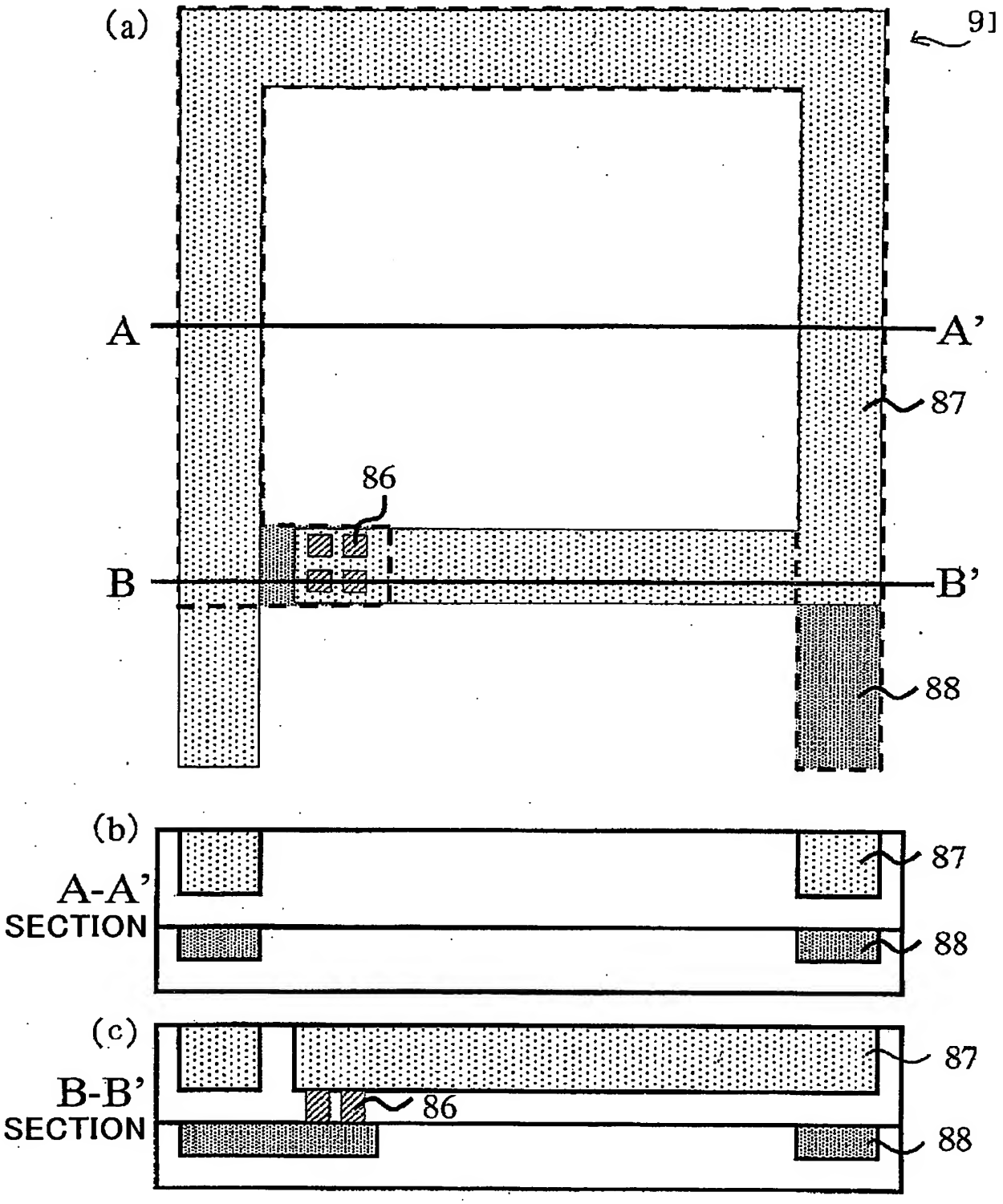


Fig. 34

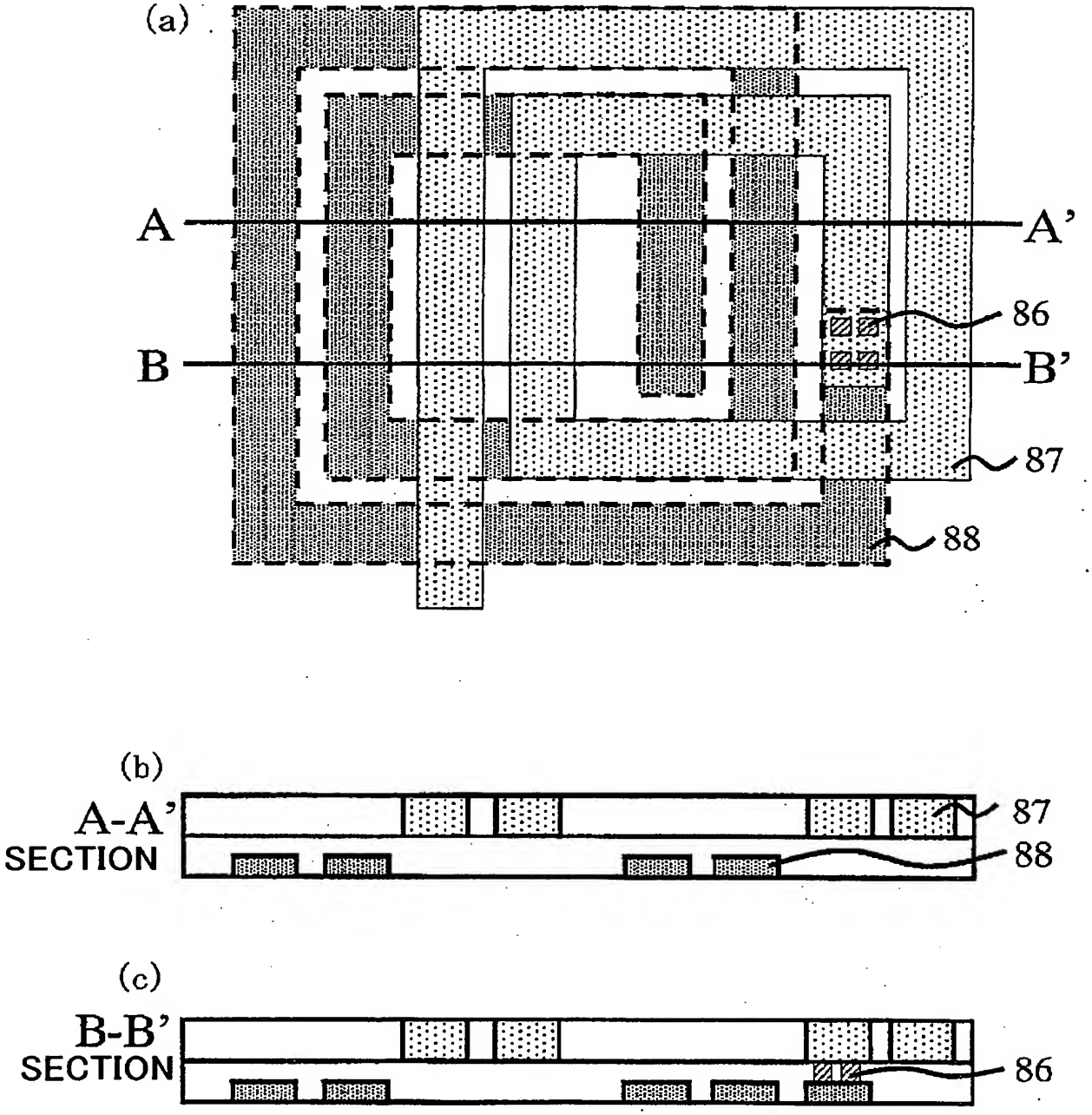


Fig. 35

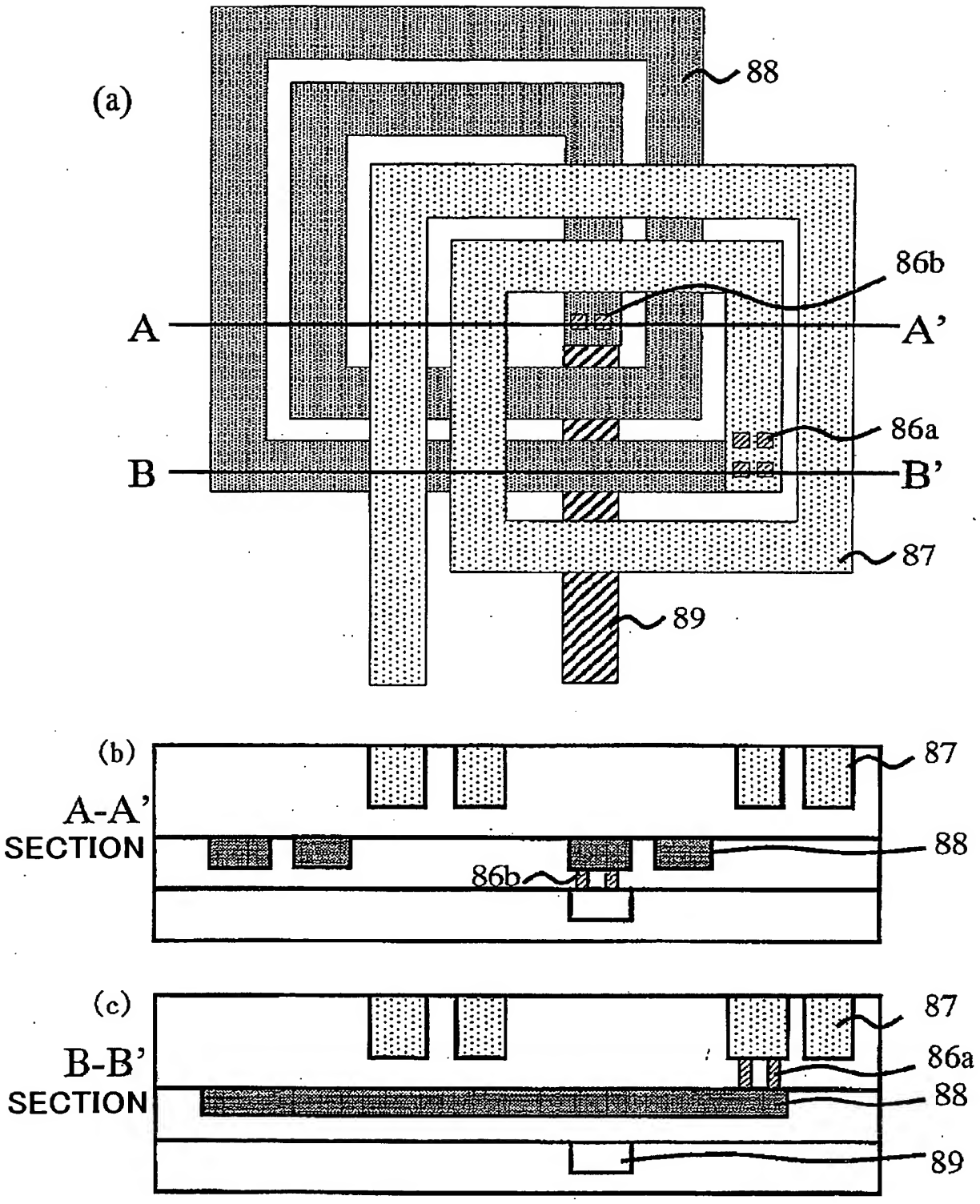

(a)
88
86b
A
A'
86a
B
B'
87
89
(b)
A-A'
SECTION
87
88
86b
(c)
B-B'
SECTION
87
86a
88
89

Fig. 36

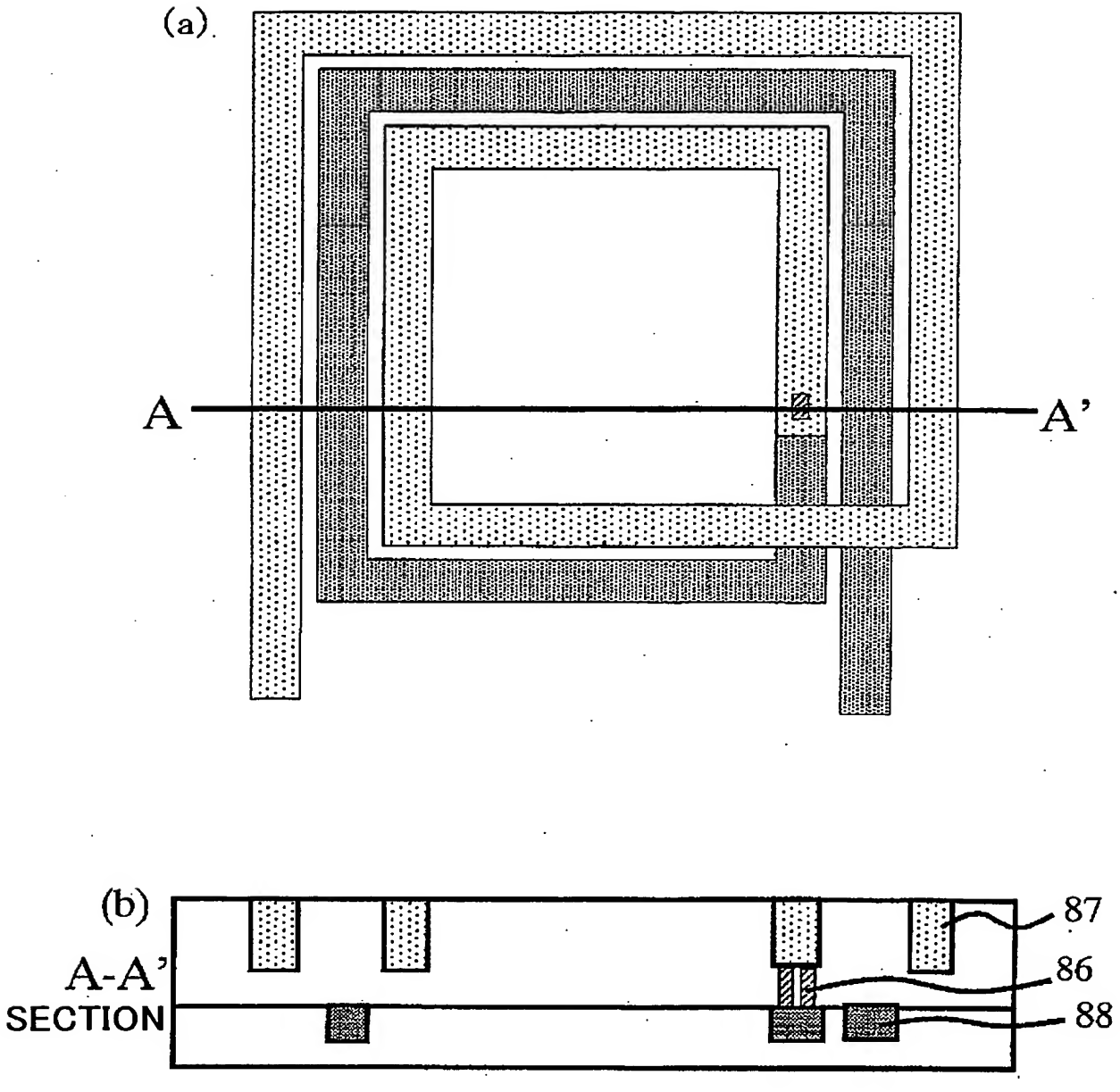


Fig. 37

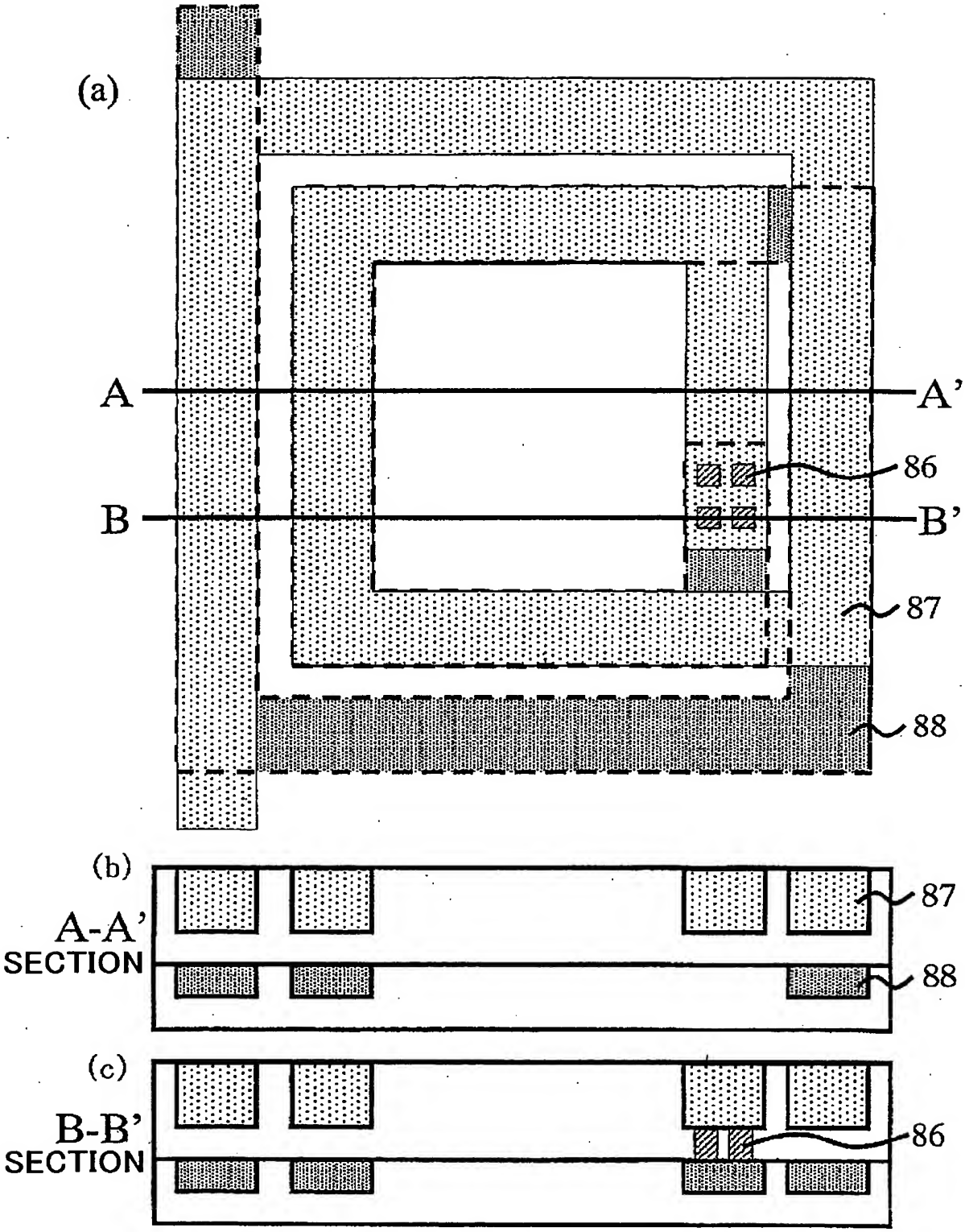


Fig. 38

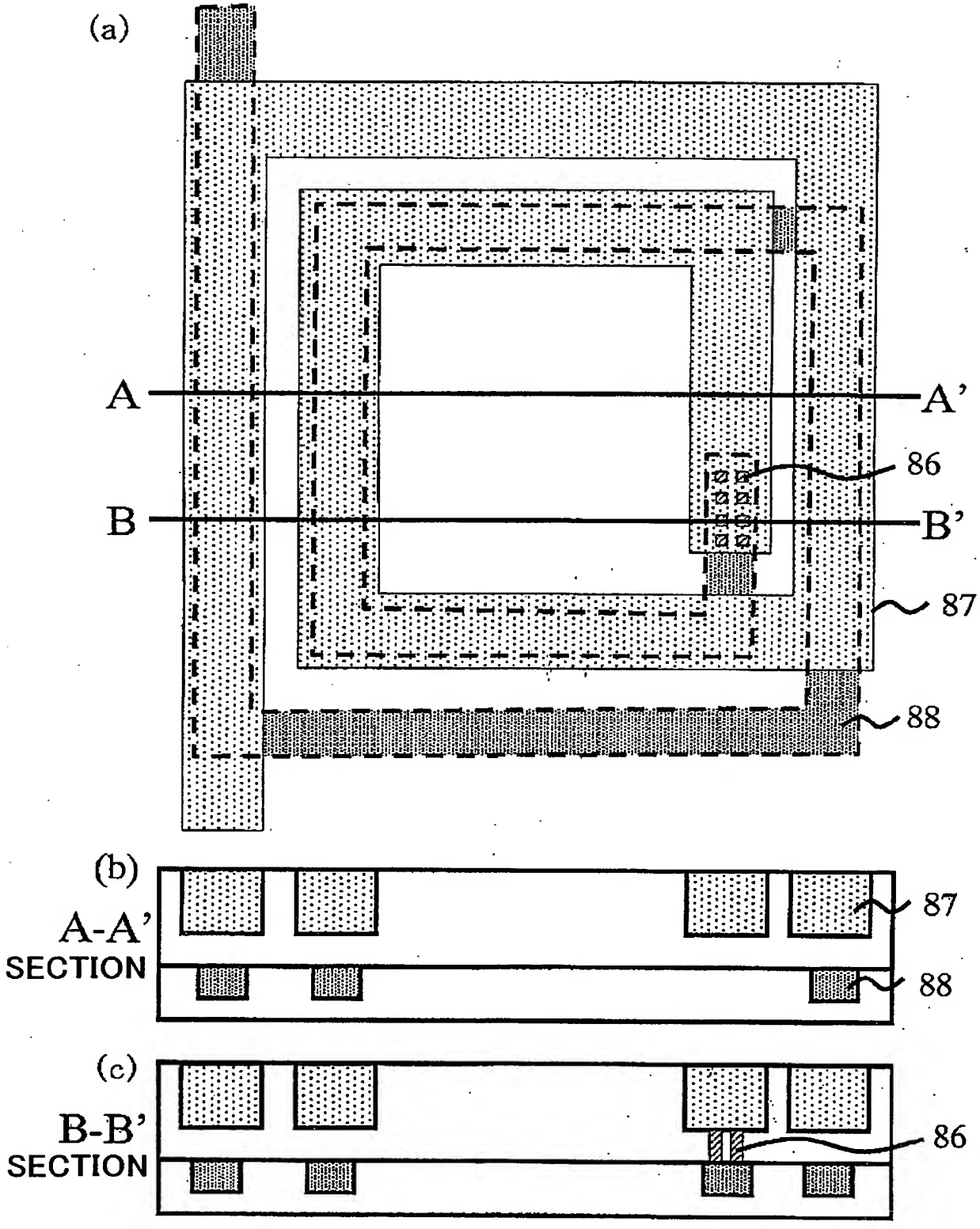


Fig. 39

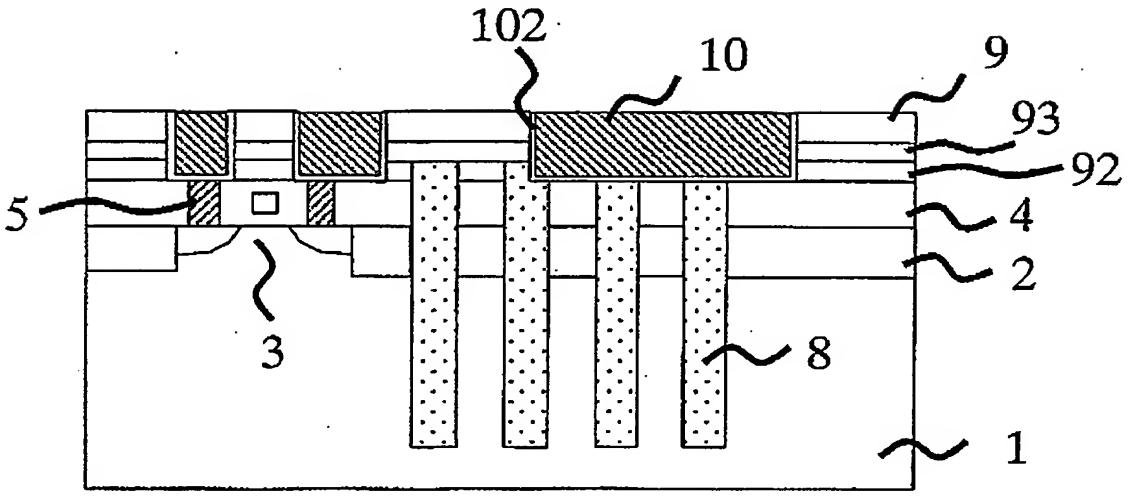


Fig. 40

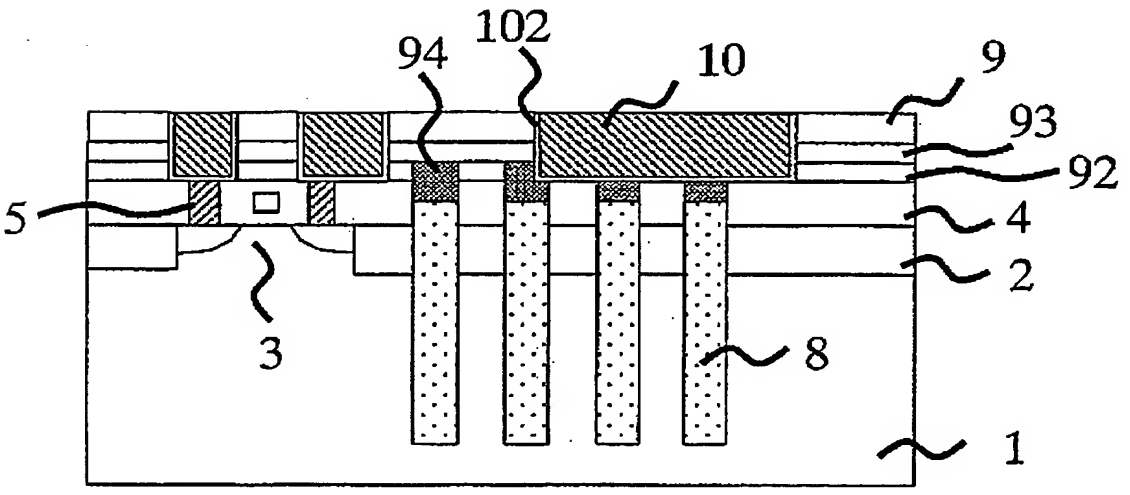
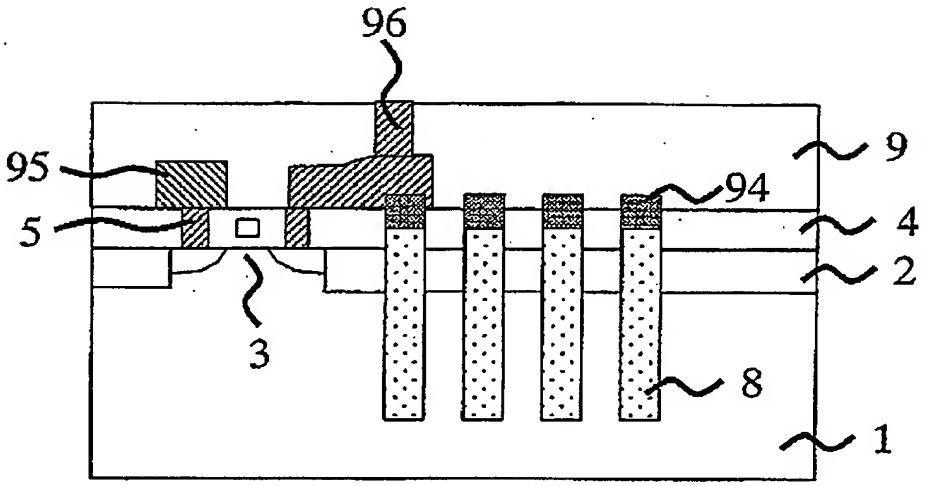


Fig. 41

(a)



(b)

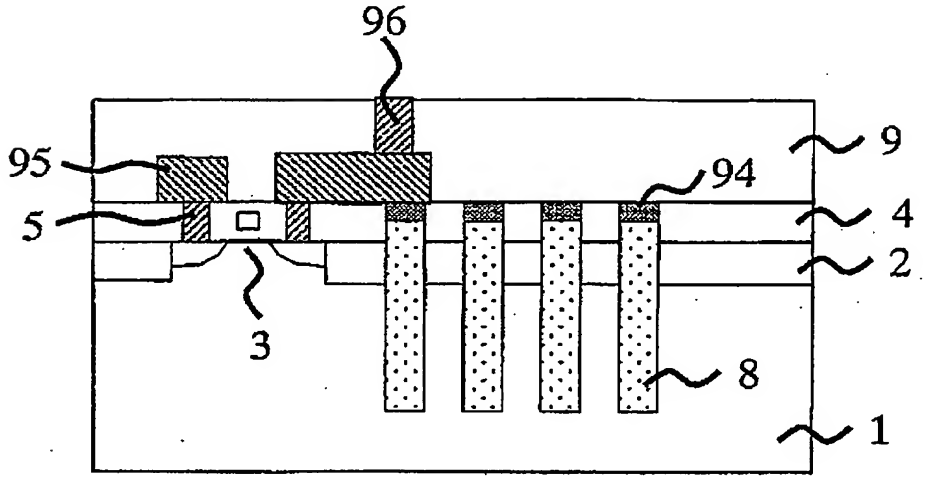


Fig. 42

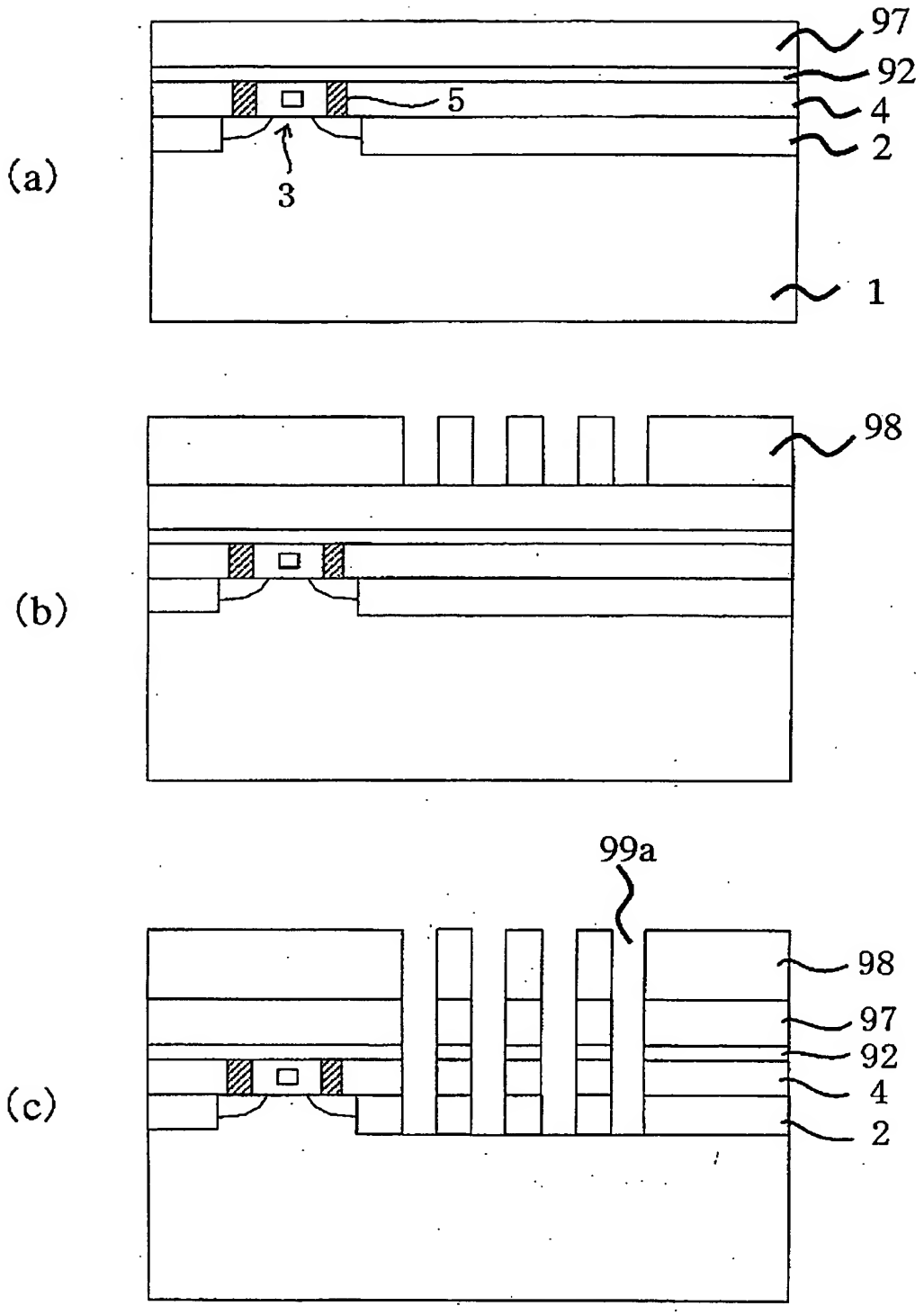
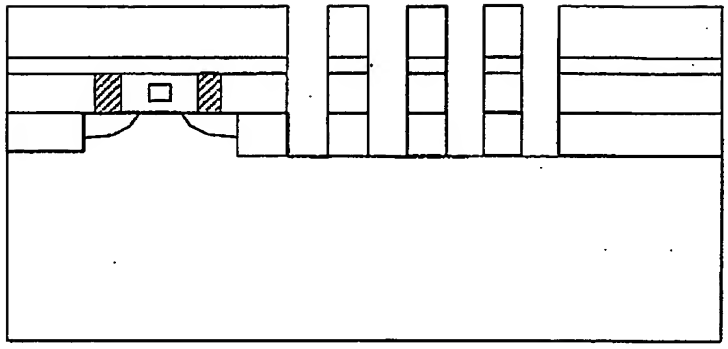
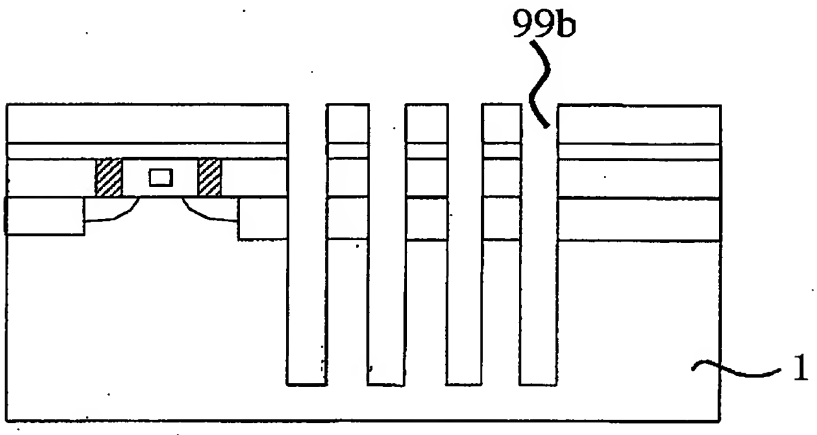


Fig. 43

(c)'



(d)



(e)

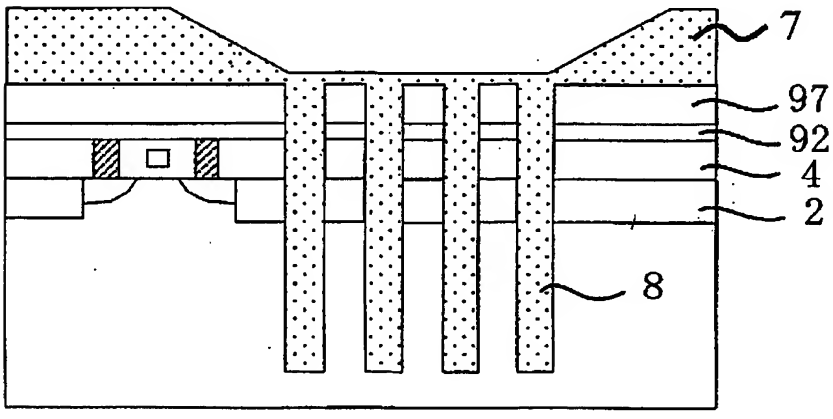
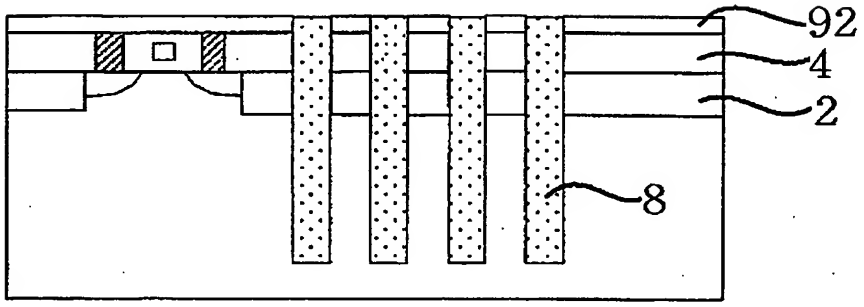
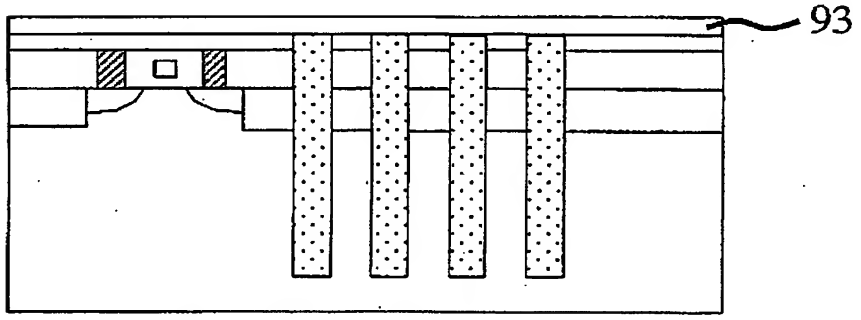


Fig. 44

(f)



(g)



(h)

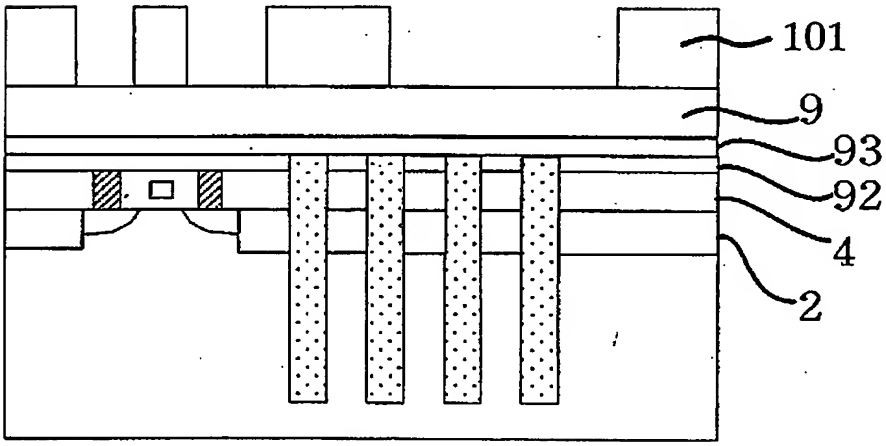


Fig. 45

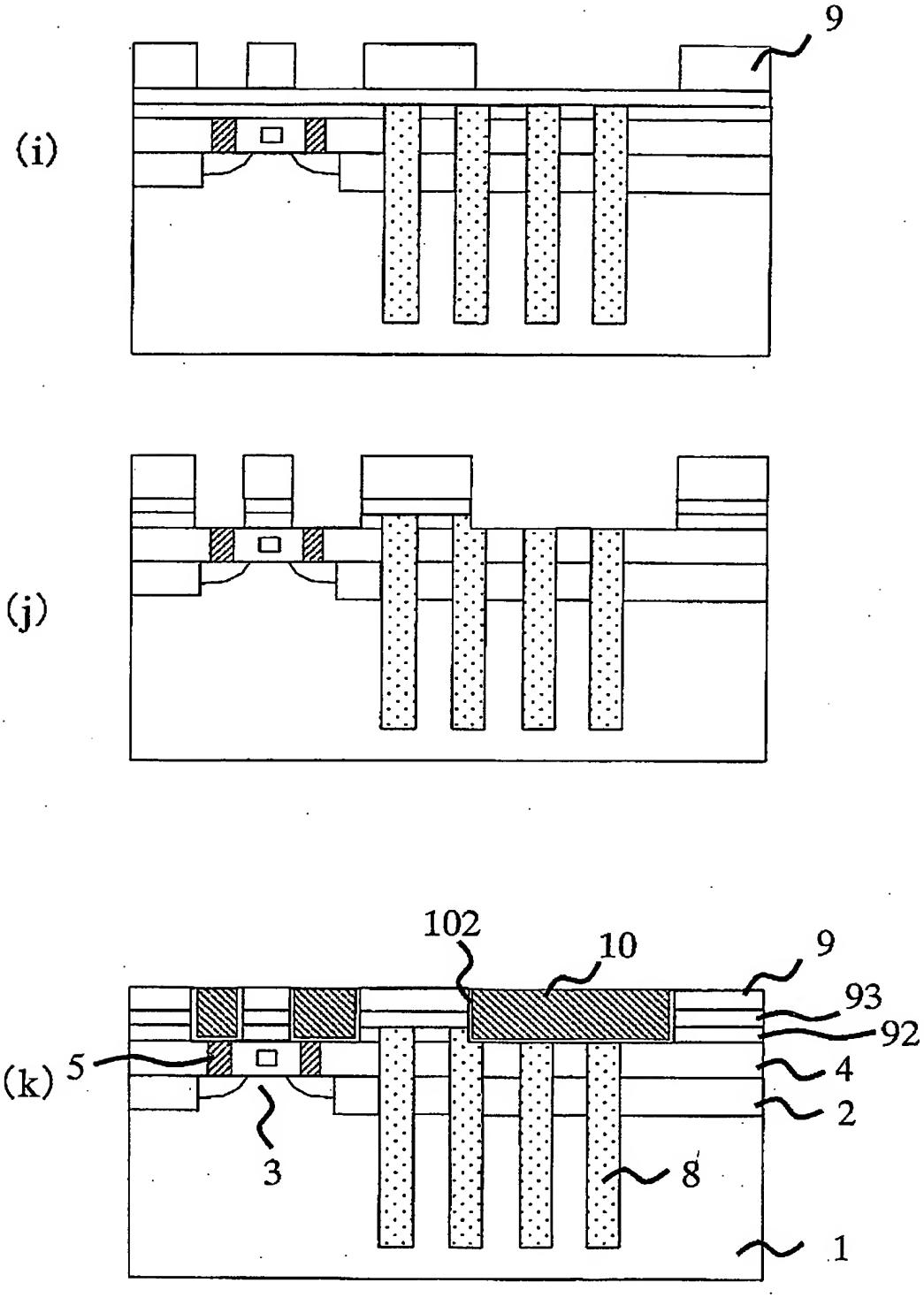
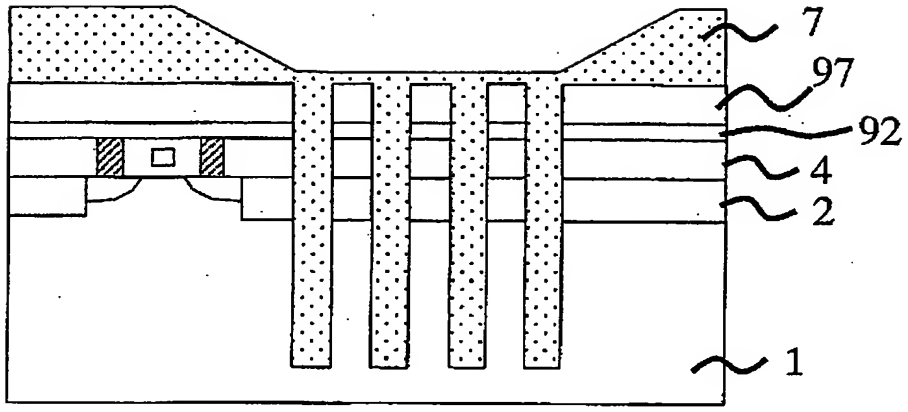
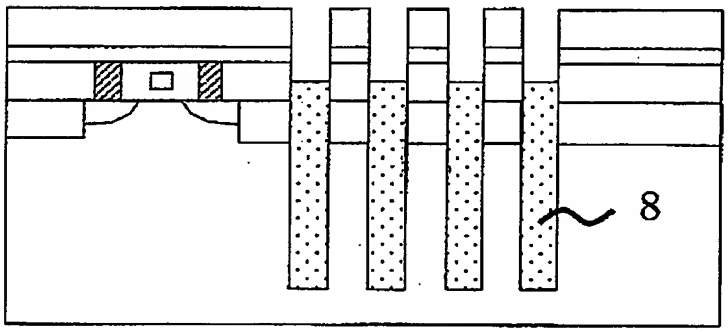


Fig. 46

(e)



(f)



(g)

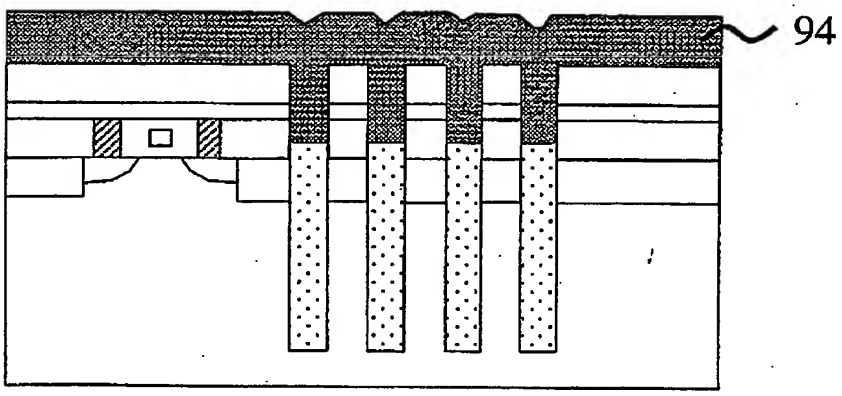
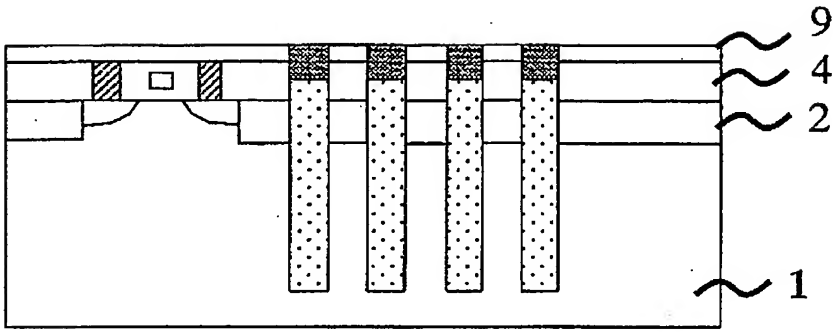
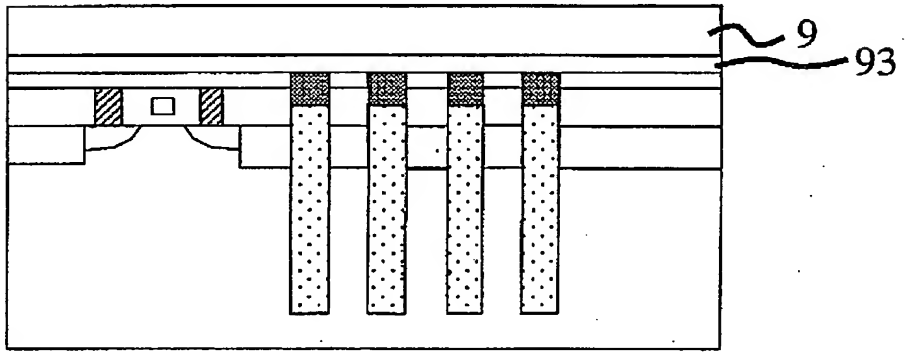


Fig. 47

(h)



(i)



(j)

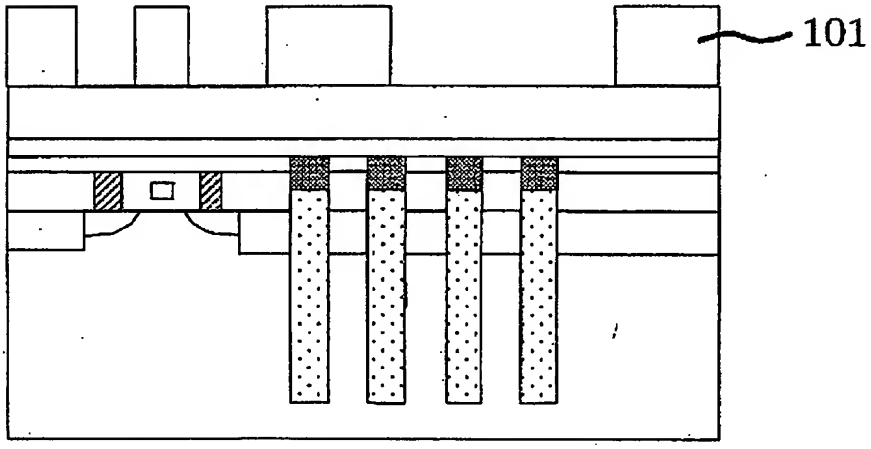
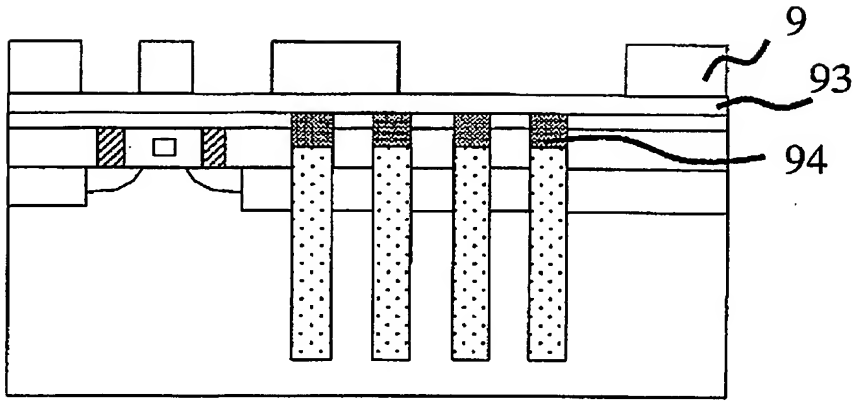
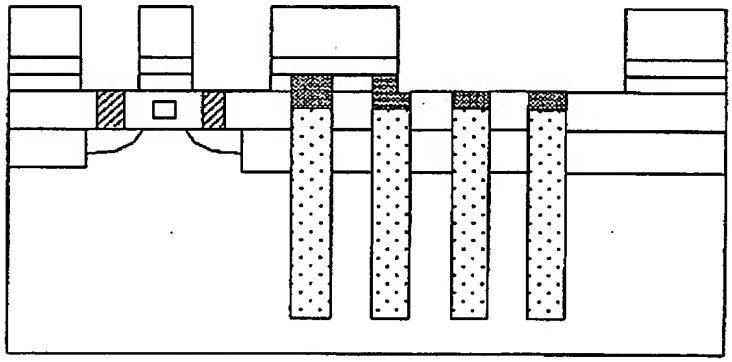


Fig. 48

(k)



(l)



(m)

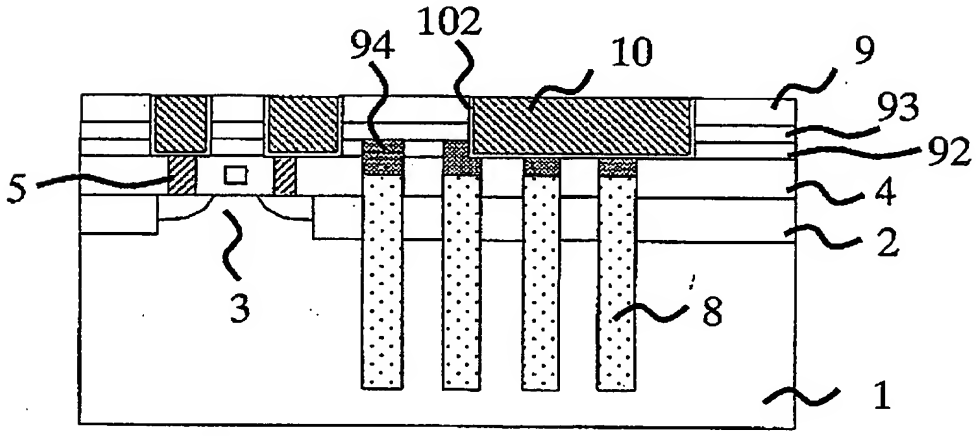
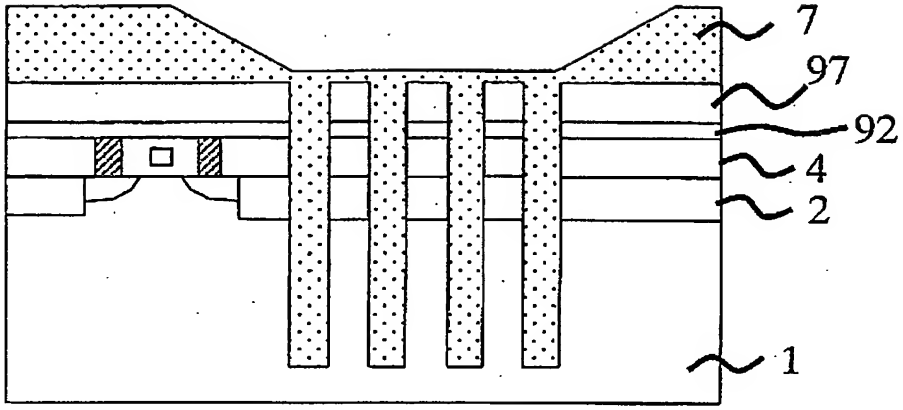
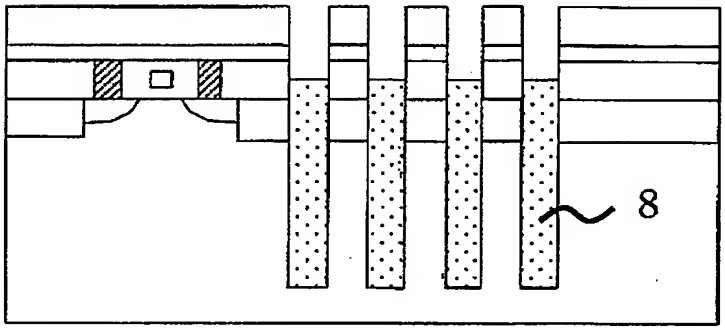


Fig. 49

(e)



(f)



(g)

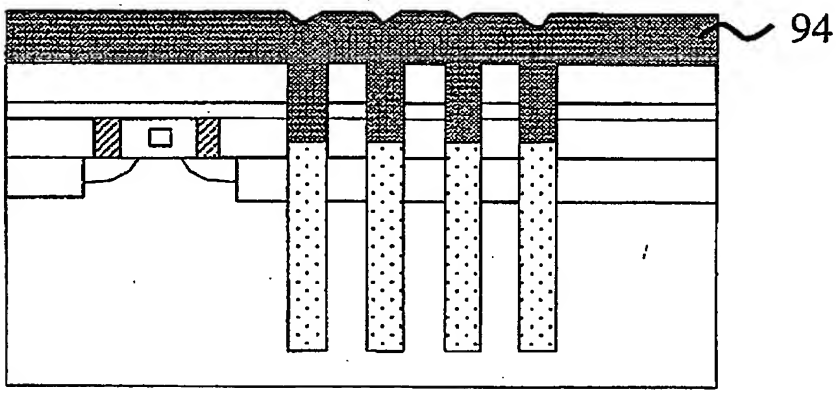
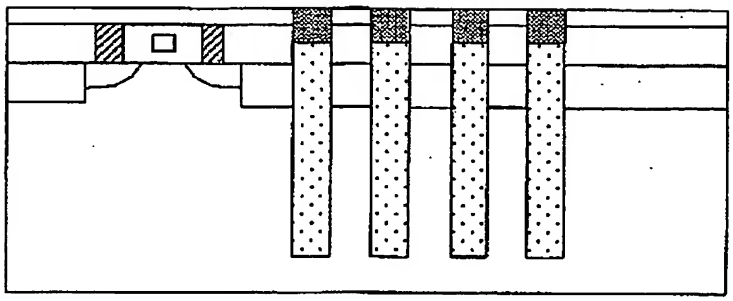
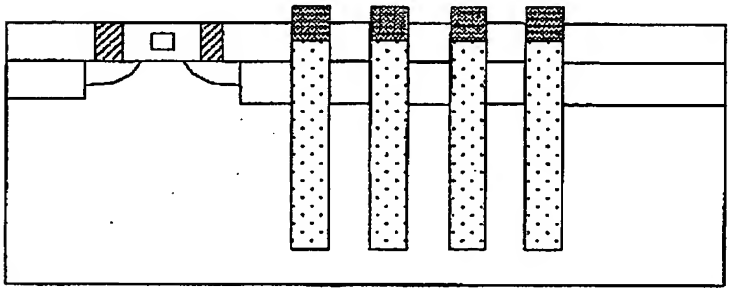


Fig. 50

(h)



(i)



(i)'

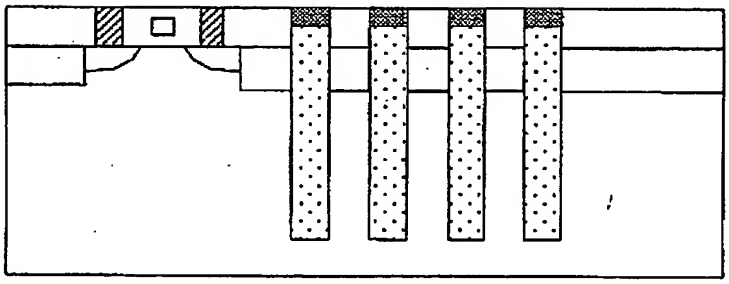
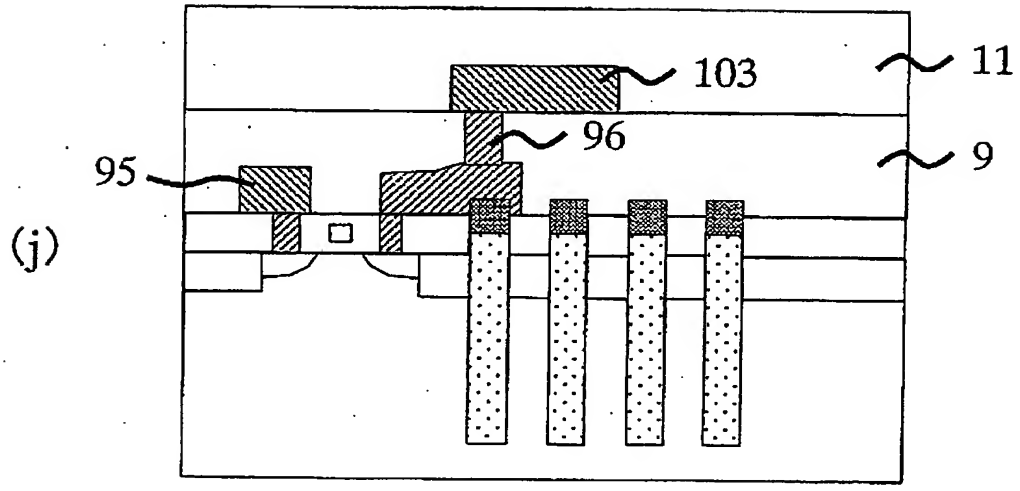


Fig. 51



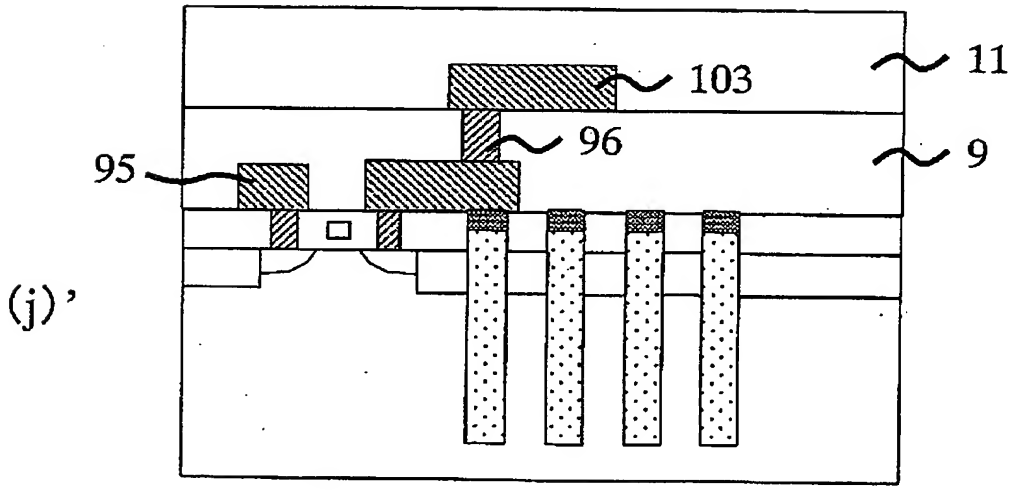


Fig. 52

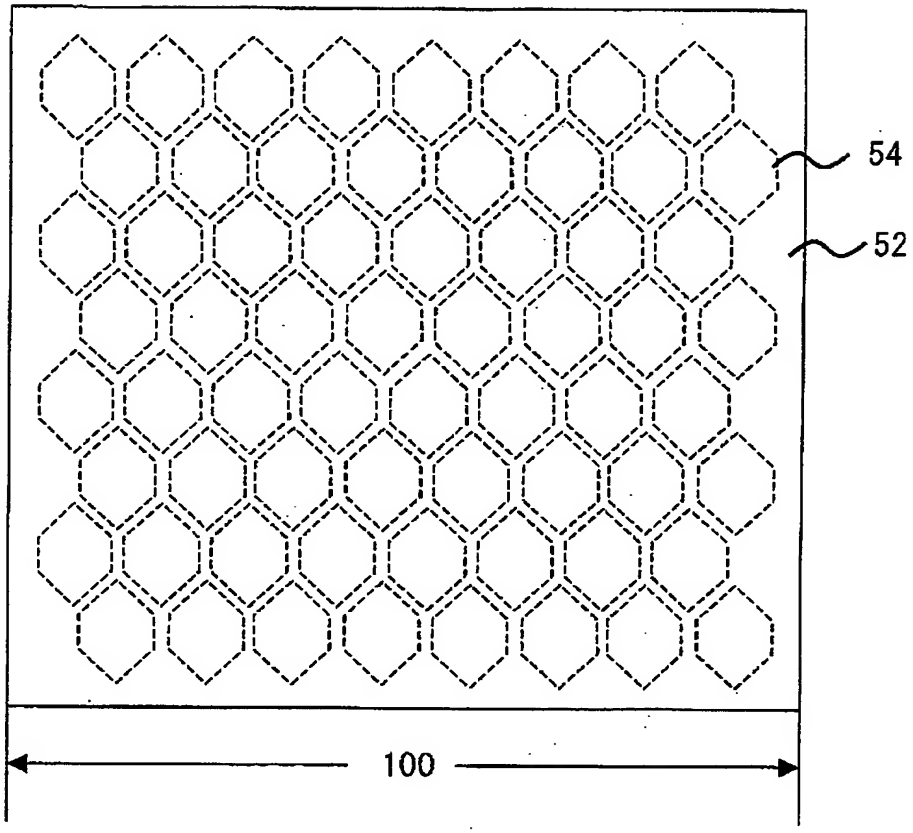
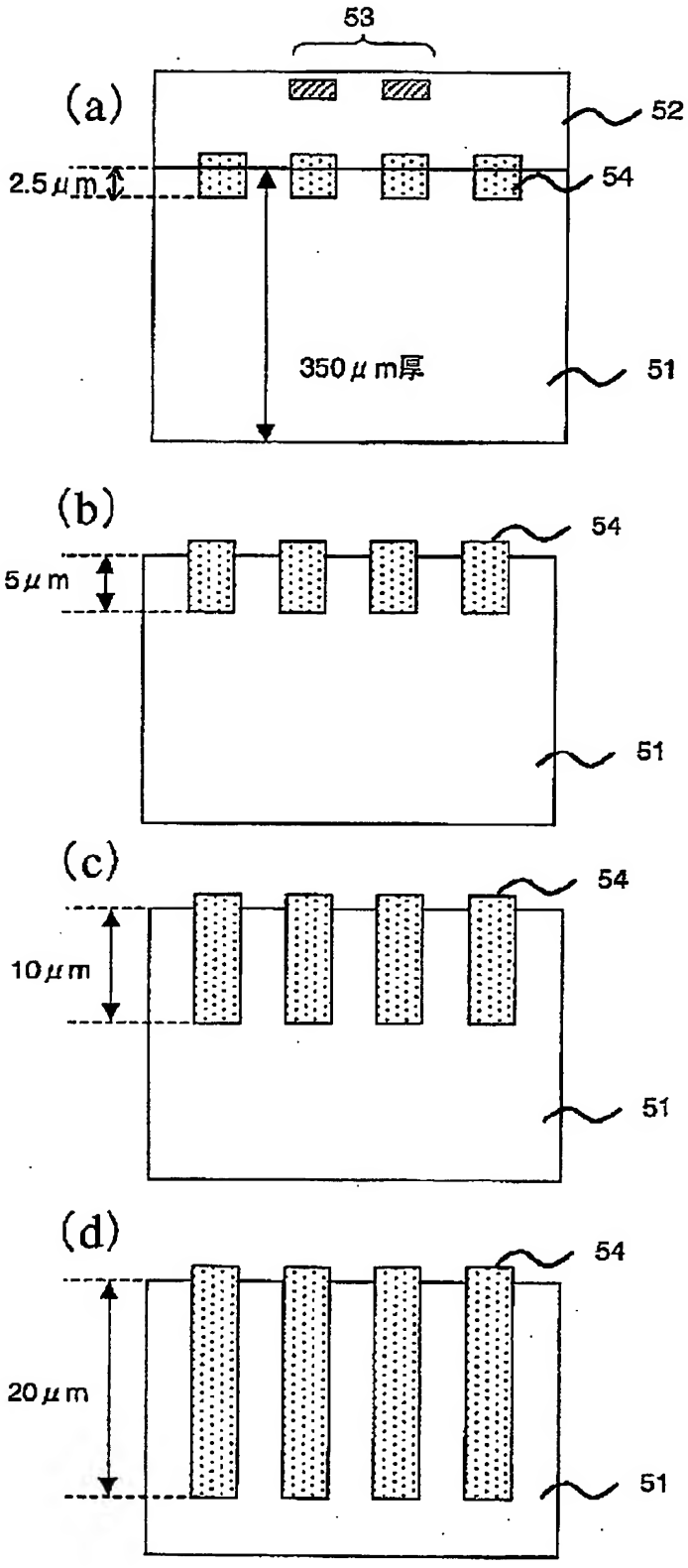


Fig. 53


53
(a)
52
2.5μm
54
350μm厚
51
(b)
54
5μm
51
(c)
54
10μm
51
(d)
54
20μm
51

(e)

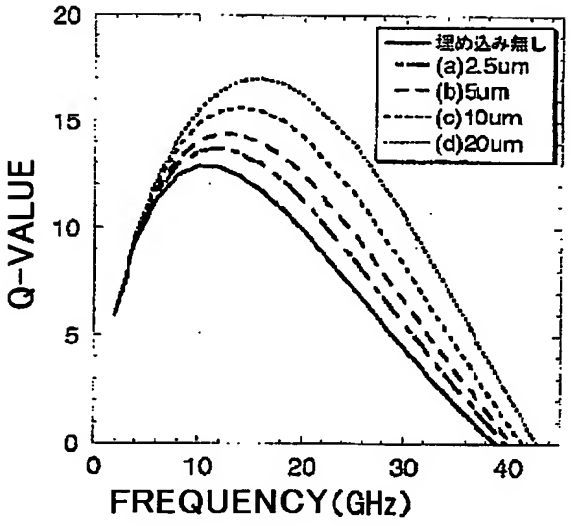
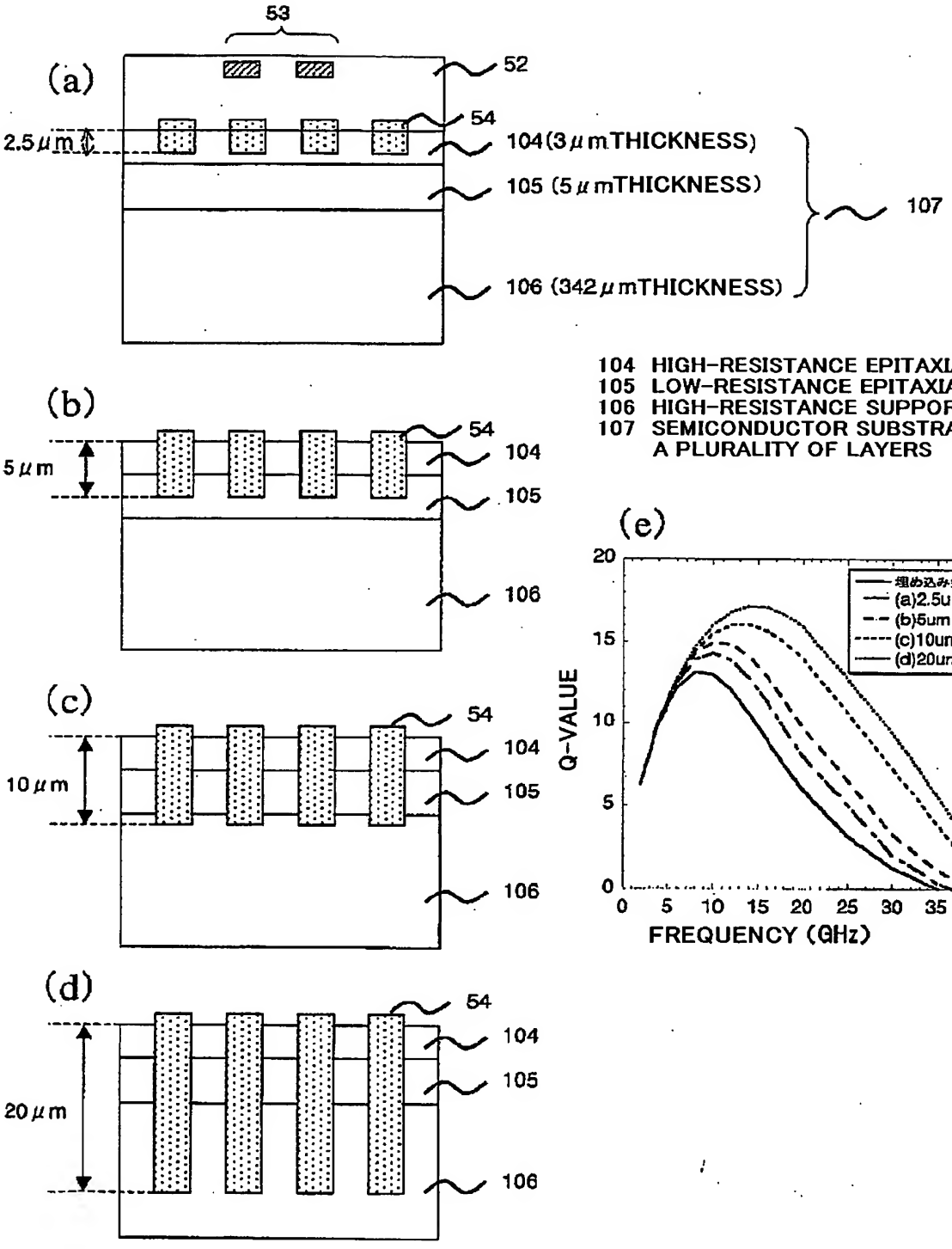

20
15
10
5
0
Q-VALUE
0
10
20
30
40
FREQUENCY(GHz)
埋め込み無し
(a)2.5um
(b)5um
(c)10um
(d)20um

Fig. 54


(a)
53
52
54
2.5μm
104(3μmTHICKNESS)
105 (5μmTHICKNESS)
107
106 (342μmTHICKNESS)
(b)
5μm
54
104
105
106
(c)
10μm
54
104
105
106
(d)
20μm
54
104
105
106
104 HIGH-RESISTANCE EPITAXIAL LAYER
105 LOW-RESISTANCE EPITAXIAL LAYER
106 HIGH-RESISTANCE SUPPORT SUBSTRATE
107 SEMICONDUCTOR SUBSTRATE INCLUDING A PLURALITY OF LAYERS
(e)
Q-VALUE
FREQUENCY (GHz)
埋め込み無し
(a)2.5um
(b)5um
(c)10um
(d)20um
0
5
10
15
20
25
30
35
40